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Measurement and control of semiconductor-insulator interface state density in AlGaN/GaN MIS-HEMTs

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Measurement and control of semiconductor-insulator interface state density in AlGaN/GaN MIS-HEMTs

（AlGaN/GaN MIS-HEMT の

半導体・絶縁体界面状態密度の評価と制御）

Gradual School of Engineering, University of Fukui

福井大学大学院工学研究科

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Chapter 1. Technology overview and motivation

Background

In the dawn of integrated circuits, the famous prediction by Gordon E. Moore was made: “The complexity for minimum component costs has in-creased at a rate of roughly a factor of two per year” [1]. By popular interpretation it means doubling of the transistor count every year. Originally even the author believed it to be only short term advancement, that would continue for a decade and possibly decrease afterwards.

Yet we are now, almost 6 decades later, referring to this prediction as a Moore’s law and with minor changes added in 1975 it still applies. Field of semiconductors and microelectronics since then was advancing exponentially, quickly approached theoretical limits of germanium and replaced it with silicon. Utilizing clever design techniques, process control and advancements in photolithography allowed us to push well into nanometer feature size with extraordinary yields [2,3]. But for high power and high frequency applications theoretical limits imposed by silicon are already a significant problem.

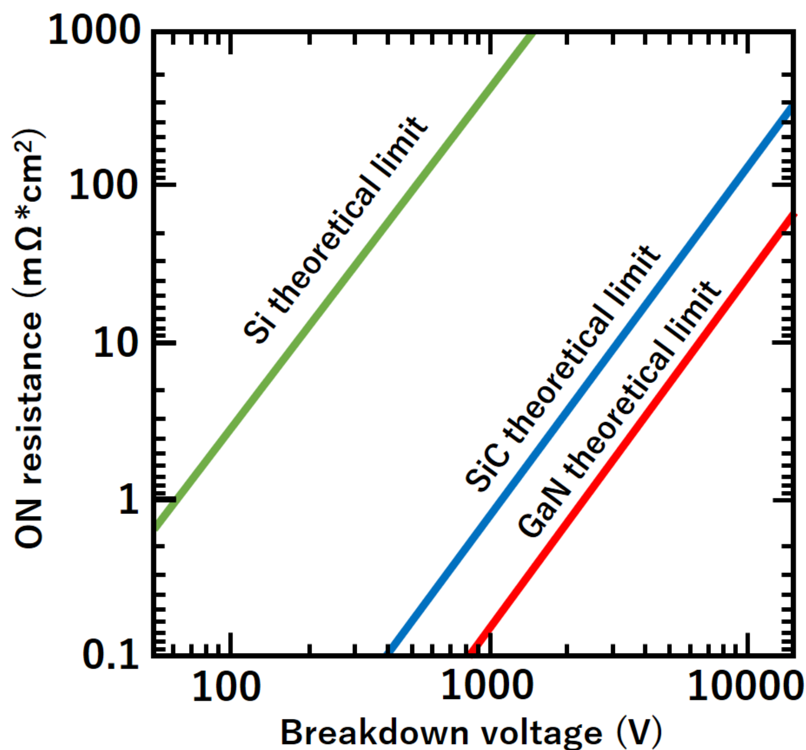

Figure 1. Theoretical limits of ON resistance and Breakdown voltage.

The root cause of this problem is best explained with limits of breakdown voltage, as on Figure 1. Breakdown voltage of the individual device scales with size, but it is a tradeoff with ON resistance. If we want to make device with low resistive losses, we will be forced to lower operating voltage and vice-versa.

Possible solution can be seen on the same figure and it is the development of more robust semiconductor materials.

Applications and advantages of Gallium Nitride

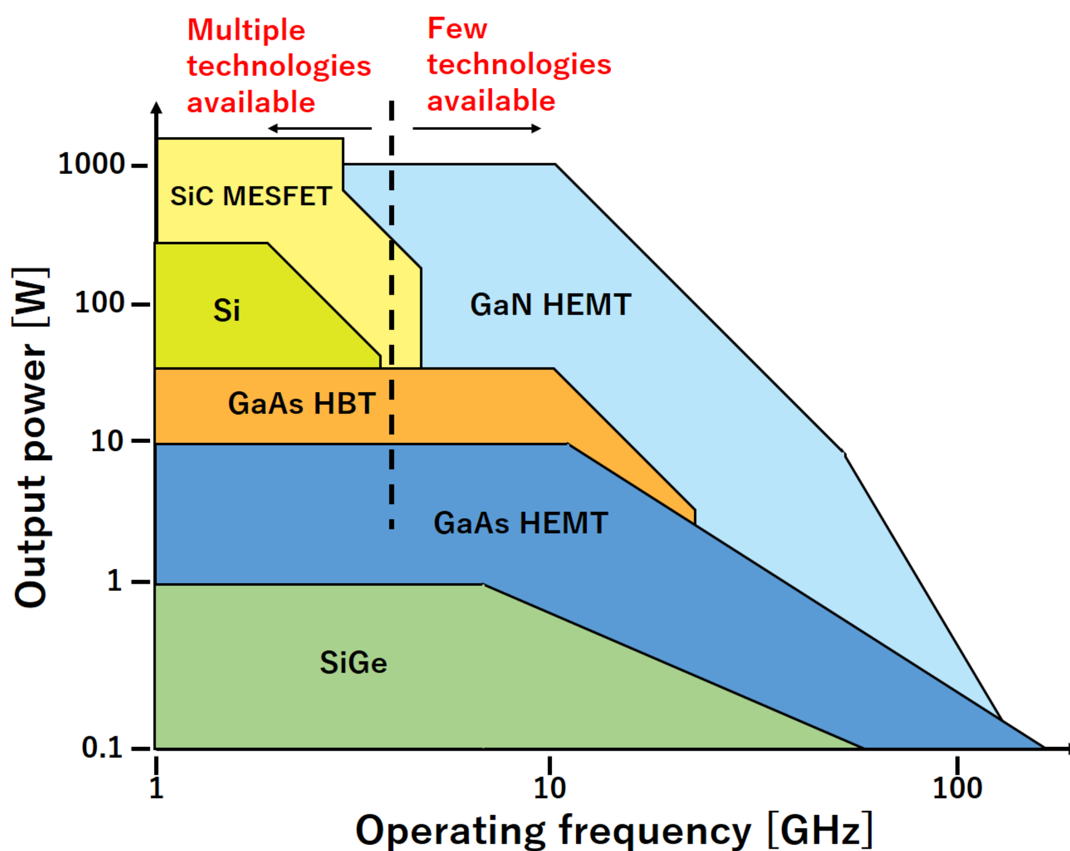

Figure 2. Device type to by application regime.

As we can see from Figure 2, that when we increase power and frequency only a couple of materials look viable. One of them is Silicon Carbide, which covers relatively low frequency but high power applications like inverters, motor driver circuits and DC-DC converters. But when moving to millimeter wave region, only GaN HEMTs can offer high output power. Possible use cases include low loss amplifiers for high speed wireless personal devices, millimeter wave radars for

self-driving cars (both in transmit and receive modes), ultra-compact high power density smartphone chargers, high power low loss amplifiers for cellular towers and so on. As we can see on the Figure 3, some applications are already being commercialized and introduced to the consumer market [4].

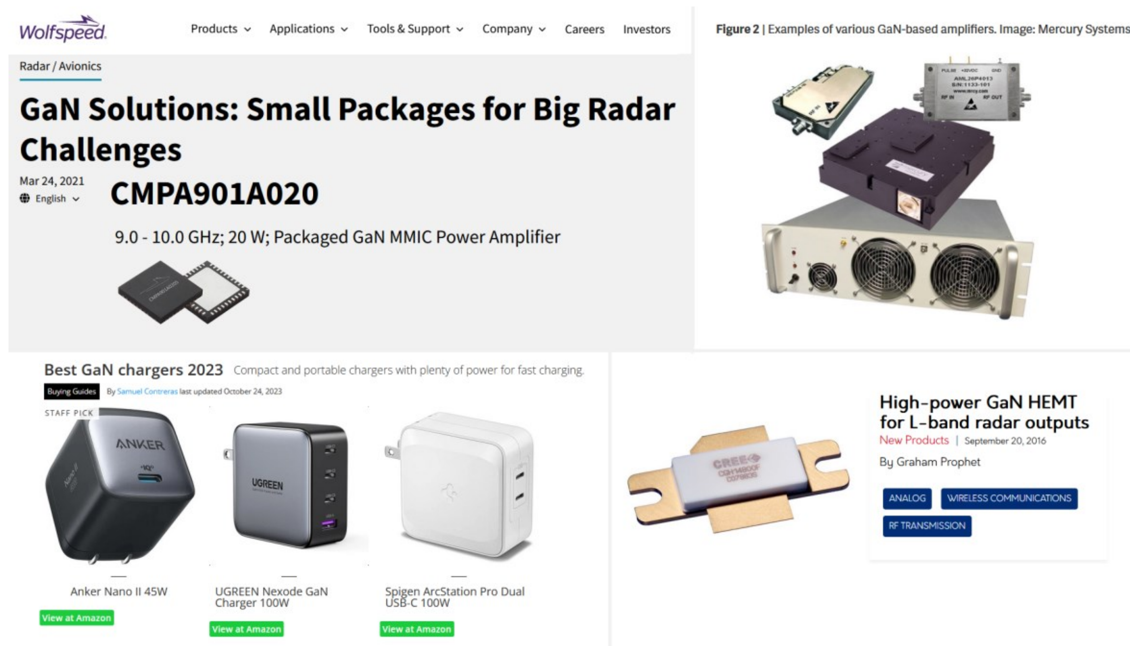

Figure 3. GaN based technologies currently on the market.

As we can see from Table 1, Gallium Nitride as a material has high breakdown field and electron velocity. And despite medium electron mobility Baliga Figure of Merit [5,6] is extremely good.

Material	Breakdown Field (MV/cm)	Electron velocity ($x10^7$ cm/s)	Electron mobility (cm^2/Vs)	BFOM
GaN	3.3	2.5	1200	3170.4
SiC	3.0	2.0	700	712.5
Si	0.3	1.0	1350	1
GaAs	0.4	1.2	8500	13.3

Table 1. Basic material properties.

This once again points at great potential of the material in low loss, high frequency applications.

Brief introduction to AlGaN/GaN HEMTs

Crystalline structure of Gallium Nitride can be seen on Figure 4. Electronegativity of Nitrogen is considerably bigger then one of Gallium, so bonding electrons are pulled towards nitrogen atom. As a result of this, Ga charges positive and N – negative. Wurtzite crystal structure is formed around large Ga by smaller N atoms, taking a shape of vertically elongated tetrahedron.

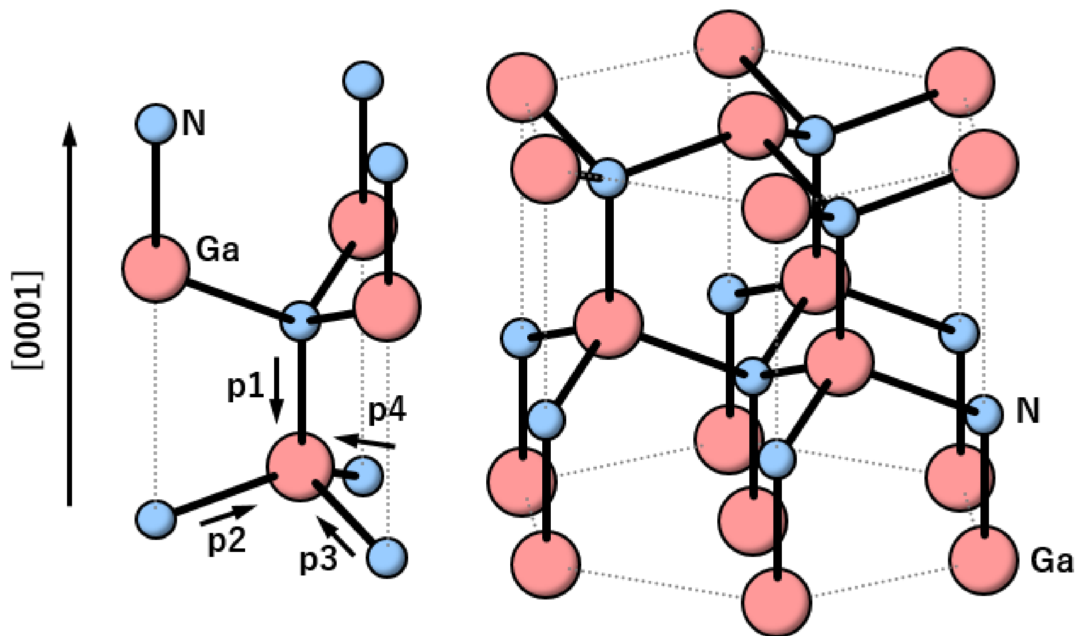

Figure 4. Crystalline structure of GaN.

As shown on the left side of the figure above dipole moments p_1 to p_4 cancel each other in all directions except vertical (c axis) and because of this asymmetry spontaneous polarization P^{SP} is created.

Figure 5 depicts that if we epitaxially grow AlGaN (which has lower lattice constant) on the surface of GaN it will cause lateral strain and vertical compression in the epitaxial layer. Compressive stress in AlGaN layer causes its piezoelectric polarization P^{PE}.

Both polarizations combined lead to the formation of net positive polarization charge at AlGaN/GaN heterostructure boundary [9]. Due to this positive charge, electrons are attracted to the interface, in a similar way if it was n-doped, and 2 Dimensional Electron Gas (2DEG) is formed [7,8].

Using this highly mobile electrons created by boundary effects as a channel we

can create High Electron Mobility Transistor or HEMT for short.

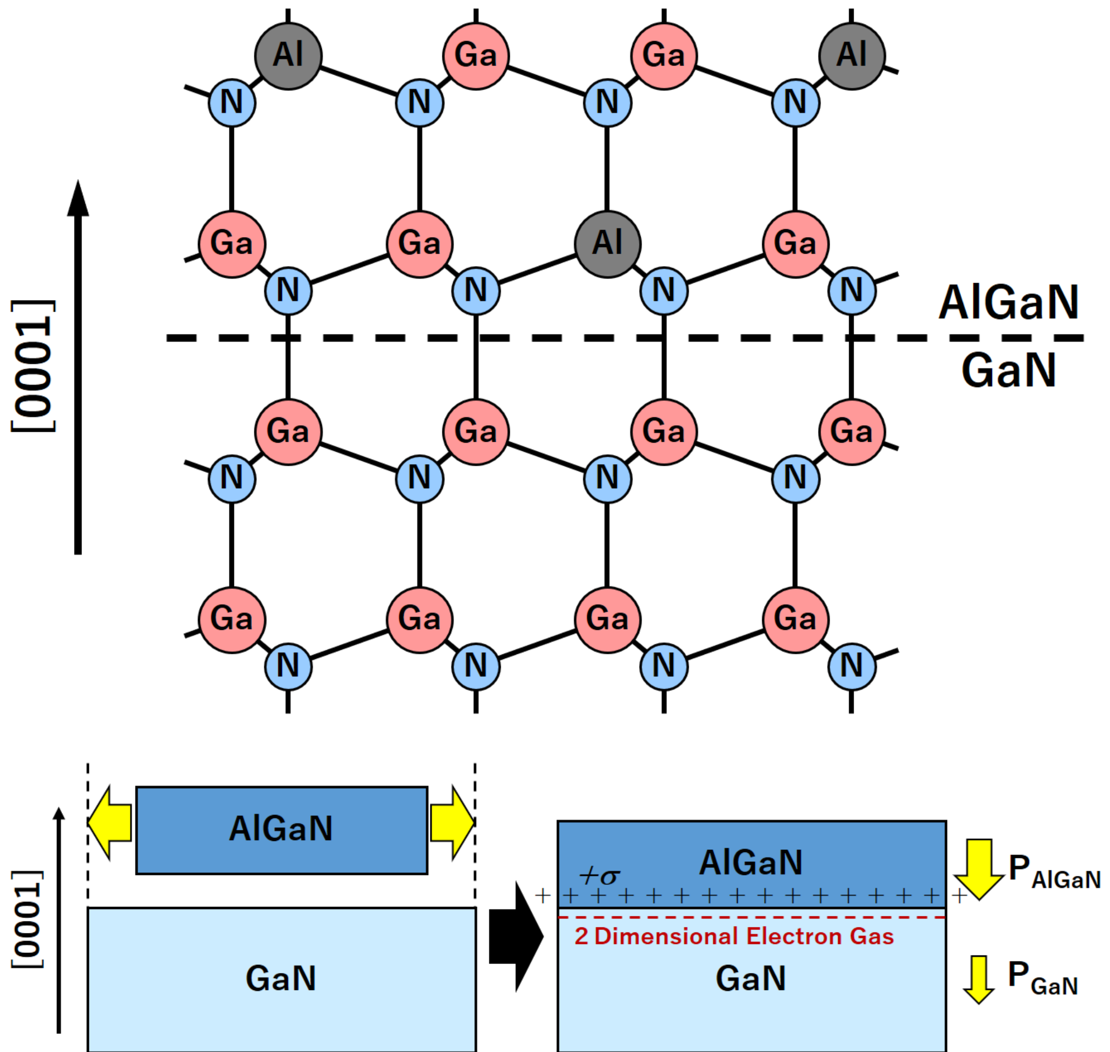

Figure 5. Epitaxial AlGaN on GaN and 2DEG formation.

For further analysis of piezoelectric polarization of AlGaN layer, as on Figure 5, we need to make a few assumptions. First is that AlGaN layer is strained uniformly without relaxation and that GaN layer compression is negligible compared to the strain effects of epitaxial AlGaN. In that case we can denote respective spontaneous polarizations as $P^{\mathrm{SP}}_{\mathrm{AlGaN}}$ and $P^{\mathrm{SP}}_{\mathrm{GaN}}$ as well as piezoelectric polarization of AlGaN $P^{\mathrm{PE}}_{\mathrm{AlGaN}}$. Then we consider the difference between polarization charges at the AlGaN/GaN boundary P and following equations can be written down

$$P = P_{\mathrm{AlGaN}} - P_{\mathrm{GaN}} \qquad (1)$$

$$P_{\mathrm{AlGaN}} = P_{\mathrm{AlGaN}}^{\mathrm{SP}} + P_{\mathrm{AlGaN}}^{\mathrm{PE}} \quad (2)$$

$$P_{\mathrm{GaN}} = P_{\mathrm{GaN}}^{\mathrm{SP}} \quad (3)$$

By combining (1), (2) and (3)

$$P = P_{\mathrm{AlGaN}}^{\mathrm{SP}} + P_{\mathrm{AlGaN}}^{\mathrm{PE}} - P_{\mathrm{GaN}}^{\mathrm{SP}} = P_{\mathrm{AlGaN}}^{\mathrm{PE}} + \left(P_{\mathrm{AlGaN}}^{\mathrm{SP}} - P_{\mathrm{GaN}}^{\mathrm{SP}}\right) = P_{\mathrm{AlGaN}}^{\mathrm{PE}} + \Delta P^{\mathrm{PE}} \quad (4)$$

where ΔP^{PE} is the difference of spontaneous polarizations of AlGaN and GaN. AlGaN can be considered a combination of AlN and GaN and depending on concentration difference its parameters would lie on the line between those two, as depicted on Figure 6.

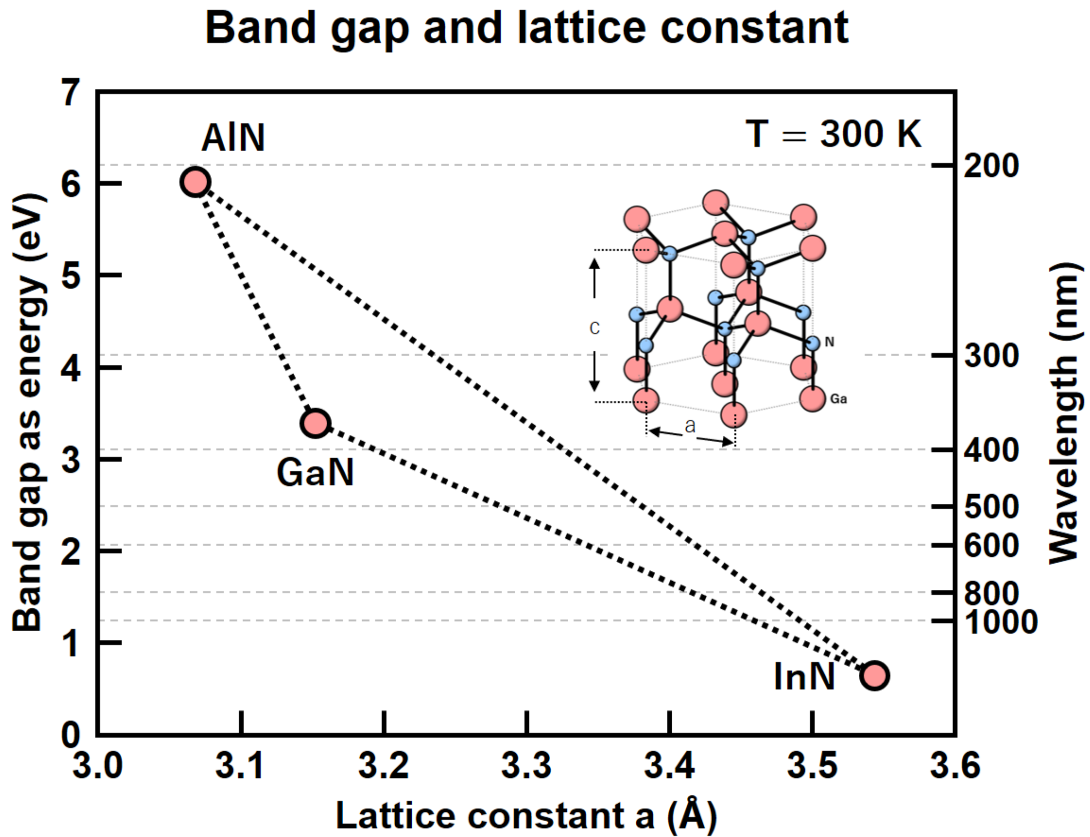

Figure 6. Band gap and lattice constant

So for pure AlN and GaN spontaneous polarization is [9]

$$P_{\mathrm{AlN}}^{\mathrm{SP}} = -0.081 \ \ (\mathrm{C/m^2}) \quad (5)$$

$$P_{\mathrm{GaN}}^{\mathrm{SP}} = -0.029 \ \ (\mathrm{C/m^2}) \quad (6)$$

and if we consider *X* as an Al content of $Al_xGa_{1-x}N$, spontaneous polarization would be

$$P_{\mathrm{Al_xGa_{1-x}N}}^{\mathrm{SP}} = P_{\mathrm{AlN}}^{\mathrm{SP}}\mathrm{x} + P_{\mathrm{AlN}}^{\mathrm{SP}}(1-\mathrm{x}) \quad (7)$$

Piezoelectric polarization $P_{\mathrm{AlGaN}}^{\mathrm{PE}}$ can be expressed with piezoelectric constant e_{ij}, compression along c axis ε_z, strain along c plane ε_x、ε_y, lattice constants in relaxed state along and perpendicular to c axis c_s, as a_s well as respective lattice constants in a strained state c_0, a_0.

$$P_{\mathrm{AlGaN}}^{\mathrm{PE}} = e_{33}\varepsilon_z + e_{31}(\varepsilon_{\mathrm{x}} + \varepsilon_{\mathrm{y}}) \qquad (8)$$

$$\varepsilon_{\mathrm{z}} = \frac{c_{\mathrm{s}} - c_0}{c_0} \qquad (9)$$

$$\varepsilon_{\mathrm{x}} = \varepsilon_{\mathrm{y}} = \frac{a_{\mathrm{s}} - a_0}{a_0} \qquad (10)$$

Here, elasticity modulus C_{13}, C_{33} can be utilized

$$\varepsilon_{\mathrm{x}} = \varepsilon_{\mathrm{y}} = -\frac{C_{33}}{2C_{13}}\varepsilon_z \qquad (11)$$

So piezoelectric polarization can be found as

$$P_{\mathrm{AlGaN}}^{\mathrm{PE}} = \left(e_{33} - \frac{C_{33}}{C_{13}}e_{31}\right)\varepsilon_{\mathrm{z}} \qquad (12)$$

and with substitution of (10) and (11) into (12) and $a_s = a_{\mathrm{GaN}}$、$a_0 = a_{\mathrm{AlGaN}}$ we get

$$P_{\mathrm{AlGaN}}^{\mathrm{PE}} = 2\frac{a_{\mathrm{GaN}} - a_{\mathrm{AlGaN}}}{a_{\mathrm{AlGaN}}}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \qquad (13)$$

In the equation above, constants in brackets are positive and polarization itself is positive (along c axis) in direction from Ga to N.

	a_0 [Å]	C_{13}[GPa]	C_{33}[GPa]	e_{31}[C/m2]	e_{33}[C/m2]
GaN	3.19	68	354	-0.34	0.67
AlN	3.11	94	377	-0.53	1.5

Table 2. Material constants for AlN and GaN [26]

Constants needed for calculation (13) can be seen in Table 2. By performing the calculation and dividing by unitary charge e, charge density can be calculated and plotted. The result can be seen on Figure 7, where Charge density at the interface was plotted against Al concentration in AlGaN layer.

Positive polarization at AlGaN/GaN interface layer forms triangular shaped potential well on GaN side of the interface [10]. To model electrons gathering in the potential well at the interface we can utilize electric neutrality condition and say the surface donor charges Q_s are present at the surface of AlGaN layer to cancel out electrons in the potential well [11].

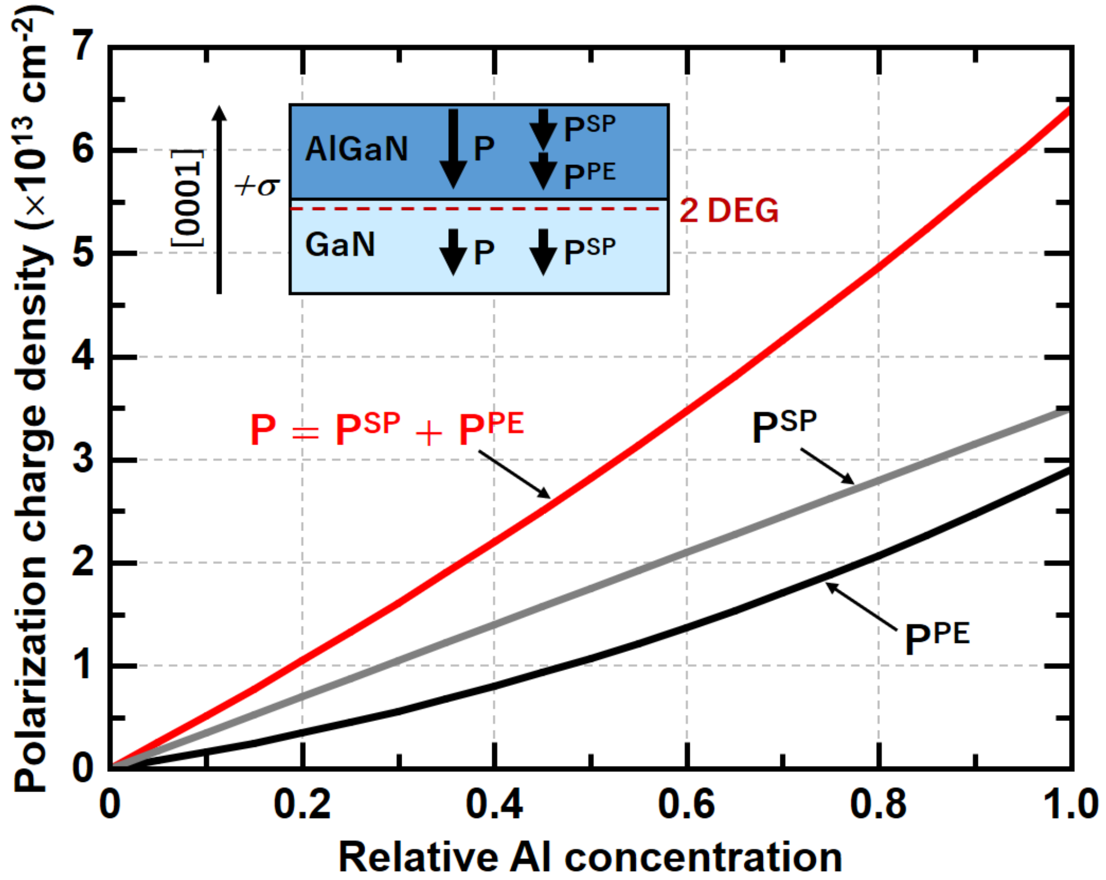

Figure 7. Polarization charge density

From that we can draw a band diagram depicting a conduction band of AlGaN/GaN heterostructure at V_{GS} = 0V, as shown on Figure 8. From the same figure we can express equation of potential and charge distribution as follows:

$$q\Phi_{\mathrm{b}} - qV_{\mathrm{AlGaN}} - \Delta E_{\mathrm{c}} + \Delta E_{\mathrm{i}} = 0 \qquad (14)$$

Here, Φ_b is a Schottky barrier height, V_{AlGaN} is a voltage applied to AlGaN layer, ΔE_c is a difference between AlGaN an GaN conduction band heights, and ΔE_i is a distance from the bottom of the potential well at the interface to Fermi level E_F. From electric neutrality condition and equation of electric flux continuity following equations can be obtained:

$$\mathrm{q}N_{\mathrm{d_s}} + \sigma_{\mathrm{p}}^{+} = \sigma_{\mathrm{p}}^{-} + \mathrm{q}n_{\mathrm{s}} \qquad (15)$$

$$\sigma_{\mathrm{p}}^{+} - \mathrm{q}n_{\mathrm{s}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}} V_{\mathrm{AlGaN}}}{d_{\mathrm{AlGaN}}} \qquad (16)$$

where $N_{\mathrm{d_s}}$ is a density of surface donors, σ_p^+ and σ_p^- are polarization charge densities, n_s is the sheet carrier density at AlGaN/GaN interface, ε_{AlGaN} and ε_0 are relative dielectric constant of AlGaN and vacuum dielectric permittivity, d_{AlGaN} is

the thickness of AlGaN layer. The resulting band diagram can be obtained with (14) and (16).

Since potential well is below Fermi-level electrons are gathering there and forming a sheet-like structure called Two Dimensional Electron Gas, or 2DEG for short.

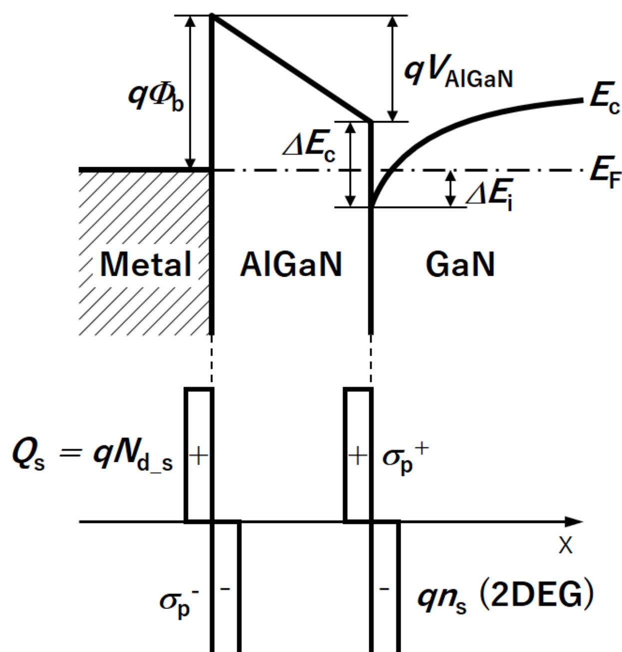

Figure 8. Band diagram of AlGaN/GaN heterostructure

When ohmic contact is obtained at Source (S) and Drain (D) electrodes and the Gate (G) in between is Schottky contact – it forms basic AlGaN/GaN MES-HEMTs structure. Cross-section is depicted on the figure below.

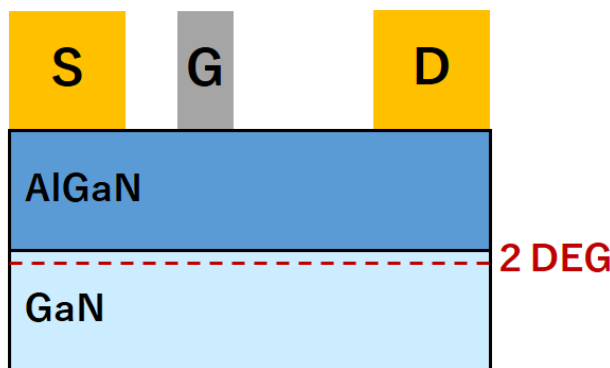

Figure 9. Cross-section structure of MES-HEMT

Density of the 2DEG under the Gate can be calculated if we solve one dimensional Poisson Equation (from gate metal towards AlGaN barrier) as follows

$$V_{\mathrm{AlGaN}} = F_{\mathrm{s}} d_{\mathrm{AlGaN}} + \frac{\sigma_p d_{\mathrm{AlGaN}}}{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}} \quad (17)$$

Here, V_{AlGaN} is the voltage applied to AlGaN layer, F_S is the strength of electric field at the AlGaN/GaN interface, d_S is the AlGaN thickness, σ_p and ε_S are polarization charge density and relative dielectric constant of AlGaN. Gauss theorem can be used to eliminate F_S as follows

$$n_s = \frac{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}}{q(d_{\mathrm{AlGaN}} + \Delta d)} \left\{ V_{\mathrm{G}} - \left(\Phi_{\mathrm{b}} + \frac{E_{\mathrm{F0}}}{q} - \frac{\Delta E_{\mathrm{c}}}{q} - \frac{\sigma_{\mathrm{p}}\ d_{\mathrm{AlGaN}}}{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}} \right) \right\} \quad (18)$$

where Δd is the distance from peak 2DEG density to the AlGaN/GaN interface

$$\Delta d = \varepsilon_0 \varepsilon_{\mathrm{AlGaN}} \frac{E_{\mathrm{F}} - E_{\mathrm{F0}}}{q^2 n_{\mathrm{s}}} \quad (19)$$

When E_{F0} is the Fermi energy at n_s = 0, threshold voltage V_{th} and n_s can be rewritten as

$$V_{\mathrm{th}} = \Phi_{\mathrm{b}} + \frac{E_{\mathrm{F0}}}{q} - \frac{\Delta E_{\mathrm{c}}}{q} - \frac{\sigma_{\mathrm{p}} d_{\mathrm{AlGaN}}}{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}} \quad (20)$$

$$n_{\mathrm{s}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{AlGaN}}}{q(d_{\mathrm{AlGaN}} + \Delta d)} \left(V_{\mathrm{gs}} - V_{\mathrm{th}} \right) \quad (21)$$

For AlGaN/GaN MES-HEMTs V_{th} usually takes negative value as the right side of the equation (20) is larger, so by applying negative voltage to the gate 2DEG channel can be depleted and transistor turned OFF.

This mode of operation is called Normally-ON (when current flows at V_{GS} = 0) and is depicted on the left side of Figure 10. Conversely, when current does not flow at V_{GS} = 0, HEMT operates in Normally-OFF mode.

When the electric field at the channel is below saturation field E_S, Drain current can be represented as follows

$$I_{\mathrm{d}} = \frac{\varepsilon_s \mu W_{\mathrm{g}}}{(d_{\mathrm{AlGaN}} + \Delta d) L_{\mathrm{g}}} \left\{ \left(V_{\mathrm{gs}} - V_{\mathrm{th}} \right) V_{\mathrm{ds}} - \frac{V_{\mathrm{ds}}^2}{2} \right\} \quad (22)$$

where I_D is the Drain Current, V_{DS} is Drain to Source voltage, W_G is the gate width and L_G is the gate length. When saturation drain voltage is applied V_{DS}=V_{DS_sat}, electron velocity at drain access region is equal to saturation velocity $\nu_s = \mu E_s$. Then, saturation Drain current can be calculated as follows:

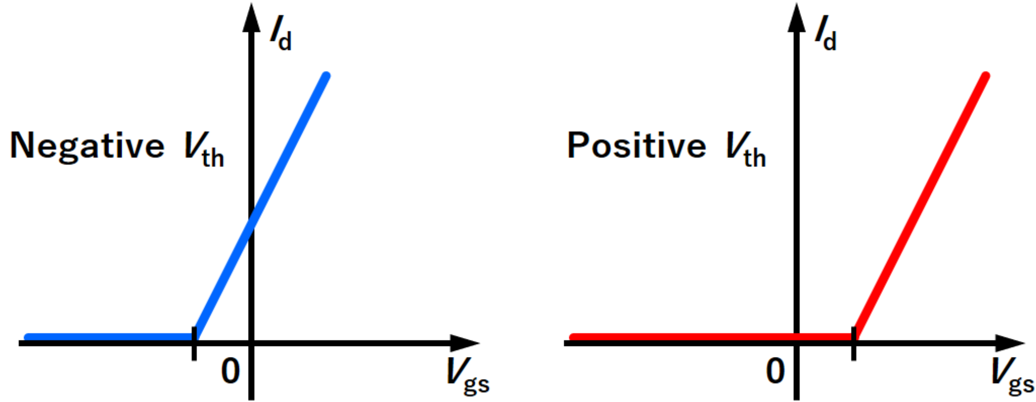

Figure 10. Example of Normally-OFF and Normally-ON operation

$$I_{d_sat} = \left\{ \frac{\varepsilon_s \mu W_g}{(d_{AlGaN} + \Delta d) L_g} \sqrt{\left(V_{gs} - V_{th}\right)^2 + E_s^2 L_g^2} - E_s L_g \right\} \qquad (23)$$

Drain Current-Voltage characteristics hence, have two distinct regions. In the linear region the increase in Drain voltage would increase the current, while in the saturation region maximum current is not dependent on the drain voltage. And in that regime increase of drain voltage beyond designed values would just cause transistor to fail catastrophically via electric breakdown and subsequent thermal runaway.

Introduction of the MIS-HEMTs

High performance Metal-Semiconductor (MES) or Schottky-Gate (SG) HEMTs discussed before were reported [13,14] before Metal Insulator Semiconductor (MIS) HEMTs [15]. Possibly due to some benefits this structure provided for early research like higher transconductance due to proximity of gate metal to 2DEG, most stable threshold voltage V_{th} and lower hysteresis due to epitaxial stack simplicity. Finally, simpler structure resulted in faster production time as well as removed additional variables related to insulator deposition from research and development process.

However, MES-HEMT structure has its own weaknesses and as technology matured over the years, advantages of insulated gate approach became apparent. One obvious advantage is depicted on Figure 11, which shows band diagrams for positively biased MES (on the left) and MIS (on the right) HEMTs. Having a gate insulator with high band gap increases Schottky barrier height, thus

prevents excessive gate leakage. This extends the range of possible gate voltages and decreases input capacitance.

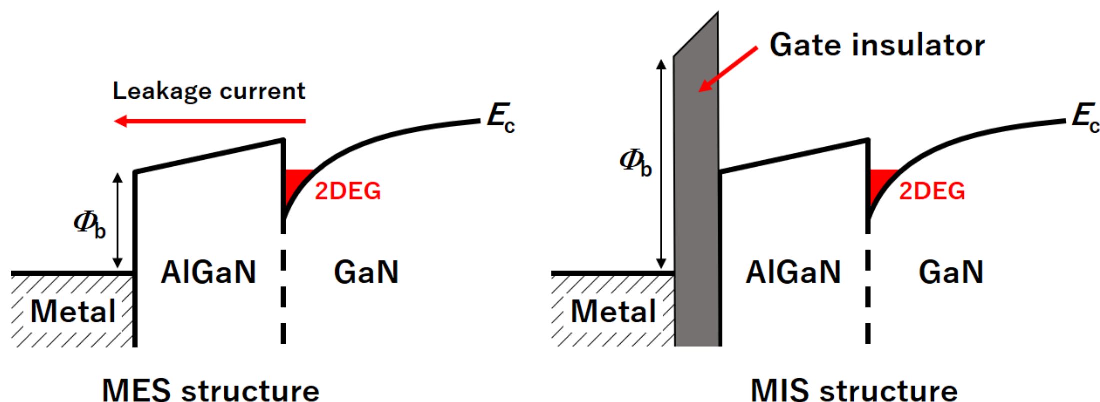

Figure 11. Band diagrams of MES and MIS-HEMT

The insulator also prevents charge injection to drain access region, so enhanced resistance to forward gate bias stress and even increased f_t [16] were reported.

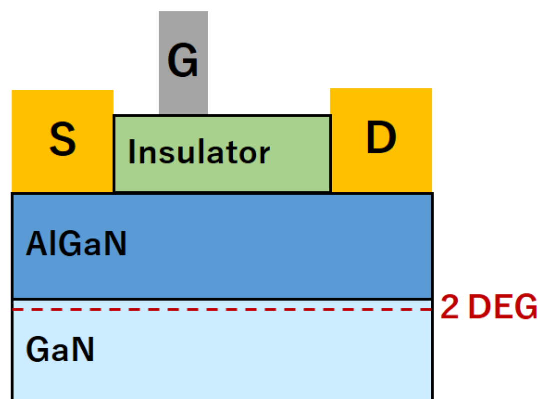

Figure 12. Cross-section structure of MIS-HEMT

Cross section of MIS-HEMT provided on Figure 12 for clarity. Usual thickness of the insulator is comparable to or lower than that of AlGaN layer.

Challenges of MIS-HEMTs

While adding an insulator layer solves some problems it also brings new challenges. Trapped bulk charges inside the layer would result in a threshold voltage shift and even hysteresis if the charge is mobile and responsive to gate sweep. Gate transconductance reduces as insulator thickness increases, so

robust materials and thickness optimization needs to be performed. Above all, it adds a new semiconductor insulator interface under the gate which inevitably causes charge accumulation.

Semiconductor-Insulator interface states

Semiconductor Insulator Interface state density was an important parameter to consider during the production of Field-Effect Transistors since the very beginning [17] and remains so to this day [18,19].

Background for interface state formation is given on Figure 13. On the left we can see simplified atomic structure adjacent to the interface. In the ideal case all dangling bonds are terminated by vacuum and no energy states exist at the boundary. In the real case however, surface atoms can rearrange, form chemical bonds with interfacing material and have non terminated (dangling) bonds.

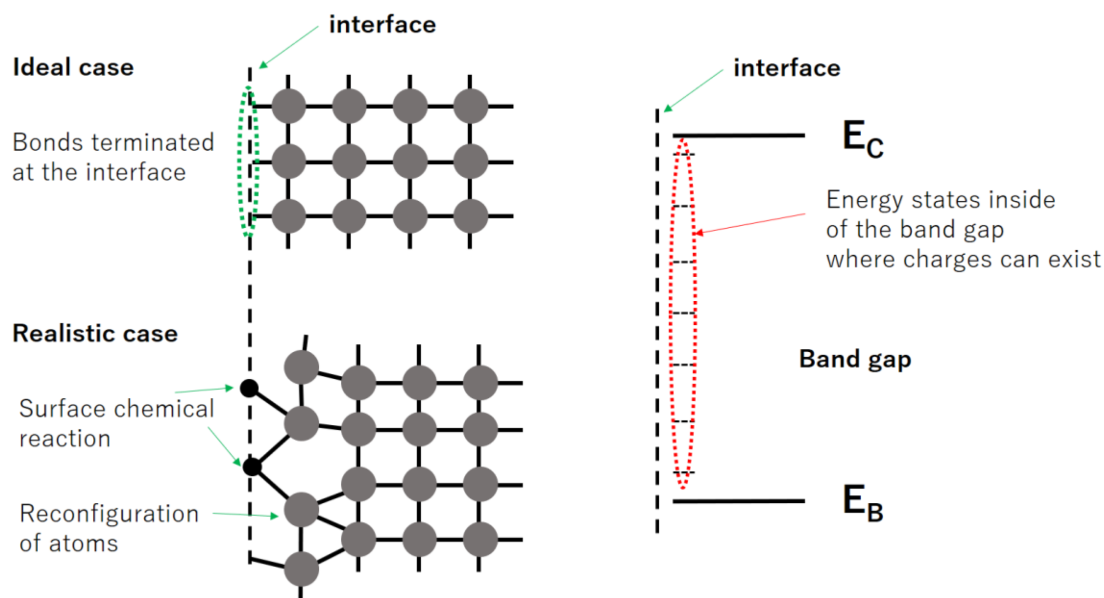

Figure 13. Physical origin of interface states

When viewed from energy perspective this forms energy states inside the band gap [20], where charges can exist, get trapped into or released from.

From early on [21] there were attempts to map energy states of these interface traps and eventually Disorder Induced Gap State model was proposed [22]. That generalized model explains surface states as thin disordered layer of semiconductor on the boundary between highly ordered semiconductor and

amorphous metal or insulator layers.

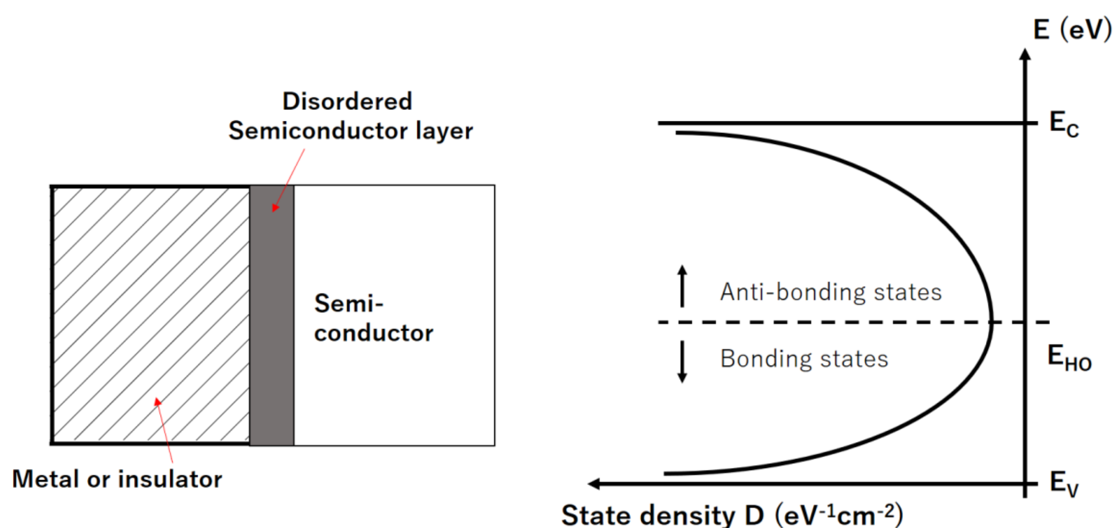

Figure 14. Simplified explanation of DIGS model [26, 27].

As depicted on the figure above two separate state density curves formed by Bonding and Anti-Bonding states create a U-shaped distribution inside the band gap with energy E_{HO} in the middle to serve as the central line where charge neutrality is achieved. It can also be interpreted as a Fermi energy of DIGS induced states.

This trap density distribution is fair for any disordered state interface, so to achieve more precision in modelling we need to include material-specific defects. For example, Nitrogen and Gallium vacancy specific trap density peaks can be simply added to the resulting distribution [23].

Possible causes of interface state density increase

Above we discussed the basic background of how interface states are formed, at the same time discussing factors influencing such effects in the real world is also important. During the semiconductor device manufacturing process (see Chapter 3) surface of the semiconductor alone undergoes multiple combinations of treatments, as well as a whole device. It is obvious that at least some of those processes would impact surface and interfacial quality of semiconductor devices.

The most straightforward effect is the surface contamination. Any leftover photoresist, carbon contamination from air, native oxide formation, organic contamination during handling and so on would cause undesired effects.

Another category is process induced defects, which appear every time the process is performed. For example, on Figure 15 we can see surface cracks (long lines at the angle of 120 degrees to each other) in AlN crystal as well as number of threading dislocation defects (short, curved lines from a single point).

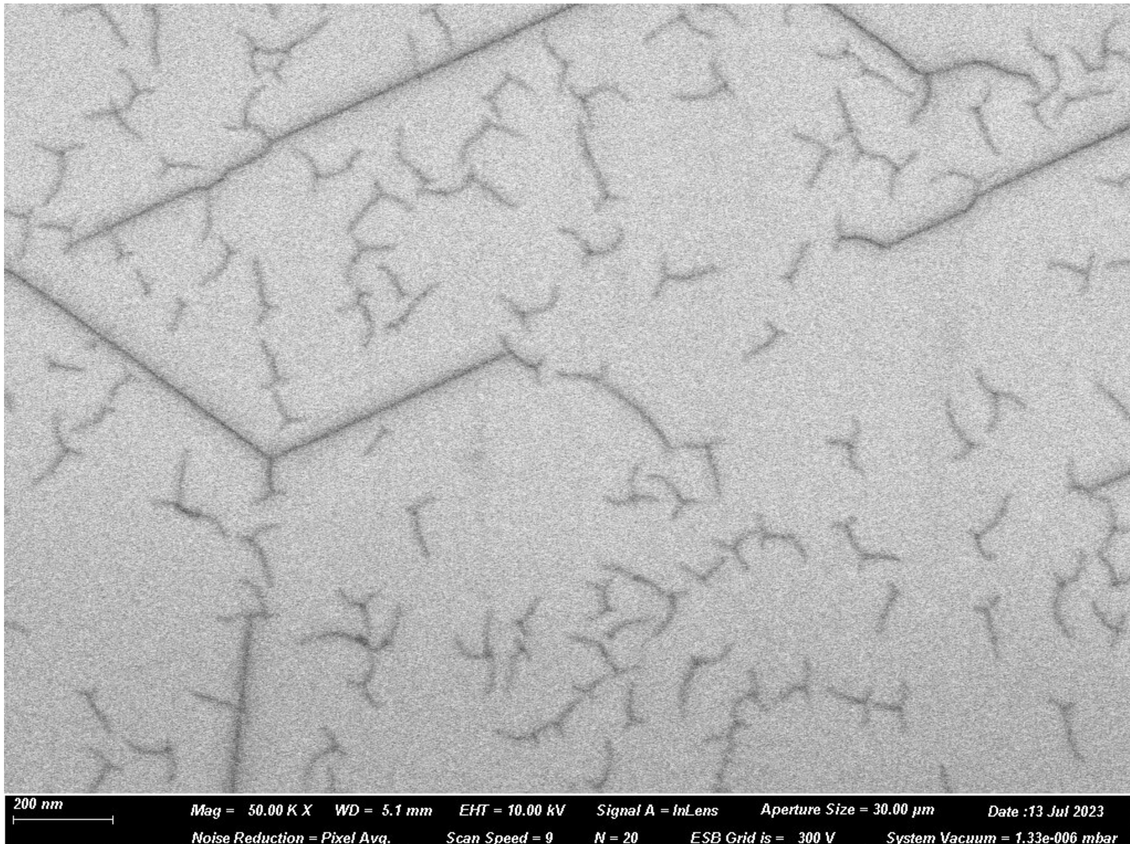

Figure 15. Surface cracks after non-optimized MOCVD growth

This is an extremely exaggerated example of epitaxial growth defects which in one shape or another are still seen in commercially available wafers to this day. Other treatments like surface passivation with argon plasma sputtering, Reactive Ion Etching, high temperature treatments during annealing or CVD depositions can cause defects or contamination as well as accelerate natural oxidation in presence of oxygen.

These processes are indispensable to semiconductor production, so it is a job of process engineer to understand and mitigate the consequences.

Effects on SG and MIS-HEMTs

Simplified structure of SG-HEMT on Figure 9 shows no insulator layers on top,

but in reality there is a protective layer of insulator on top of the device, as depicted on Figure 16. This is called passivation layer and is used to prevent surface contamination as well terminate and stabilize surface bonds of the semiconductor.

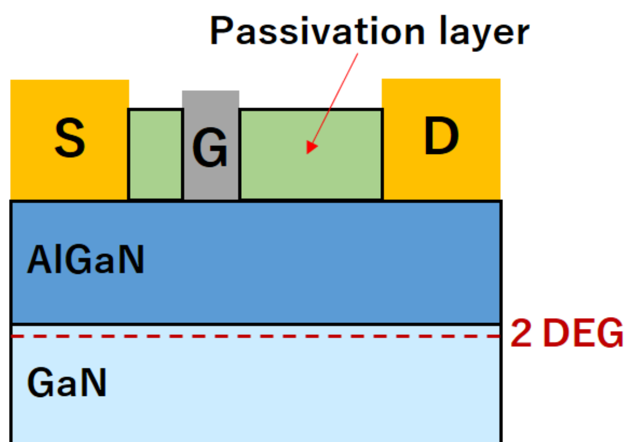

Figure 16. Passivated MES-HEMT

This means that even though SG-HEMTs do not have MIS interface under the gate electrode, interface induced effects still affect the performance of the device.

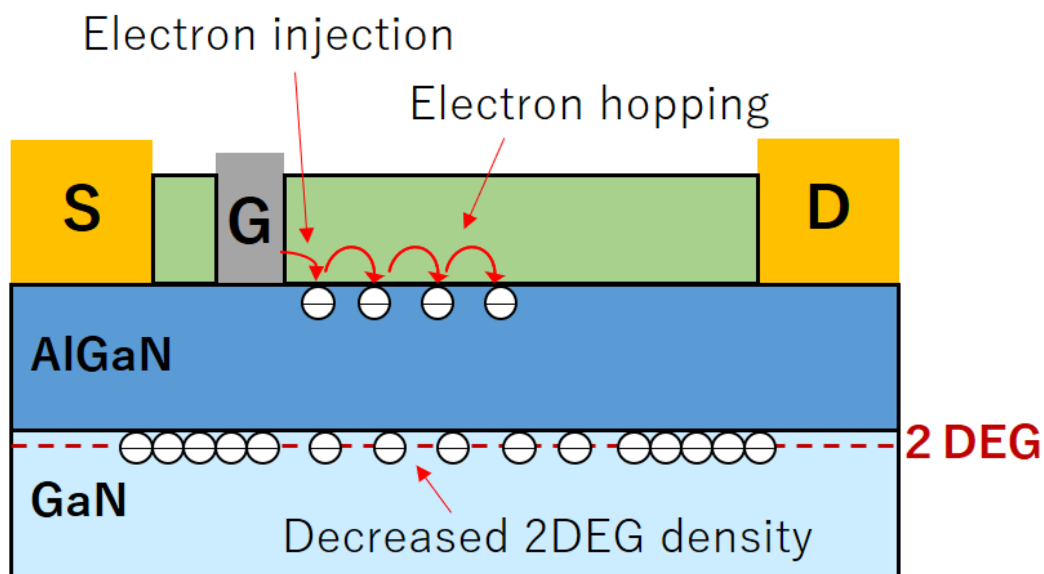

Figure 17. Interface state related effects in HEMTs

Those trap-related effects are depicted on Figure 17, above. Specifically related to SG-HEMTs, electrons can be injected into the interface at the drain access

region. In MIS structures the effect is also present, but it is not as strong due to high resistance of insulating layer. Injected electrons can utilize trap hopping mechanism [24,25] to propagate towards the drain electrode. This at first decreases the density of 2DEG, because negatively charged interface acts as “virtual gate”. For the operating device it would mean rise in ON-resistance and increased heating due to losses. Finally, as charge at the virtual gate increases, effective gate-drain distance decreases and so does the breakdown voltage. Eventually it might decrease below applied voltage and cause a failure of the transistor.
Finally, when transistor is turned ON it would take time to de-trap occupied states, so ON-resistance would be higher than normal, i.e. current collapse or dynamic ON resistance problem.

Motivation for this research

This research started with fabrication and assessment of high frequency AlGaN/GaN HEMTs with both SG and MIS structures. Some work was done to simulate and extract numerical models of fabricated devices. This opened a whole new perspective on how device characteristics can be profoundly influenced by seemingly simple structural changes.

By extension it also meant that by tweaking and optimizing core methods and technologies of production we can maximize the impact of our research. As discussed before, Semiconductor-Insulator interfaces are present in both AlGaN/GaN SG and MIS-HEMTs regardless of designed use-case. Hence, sizable improvement in interfacial quality would significantly improve performance of many types of AlGaN/GaN based devices, even if they were not considered directly in this work.

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Chapter 2 D_{it} evaluation methods

Interface analysis is by definition a difficult task to accomplish non-destructively, because we need to inspect a boundary between two not necessarily transparent or conductive solids. Over the years there were a number of methods [1,2,3] developed to help us estimate interface state density in electron devices. In this chapter I will introduce some of them and discuss their respective benefits and drawbacks.

Derivation from transfer curve and subthreshold swing

This method utilizes transfer curve measurements of MIS-HEMT, as on Figure 1, to estimate the amount of interface states in the insulator-semiconductor interface. Transfer curve measurement itself is defined as a voltage sweep of V_{GS}, while V_{DS} remains constant and I_D is being measured [1].

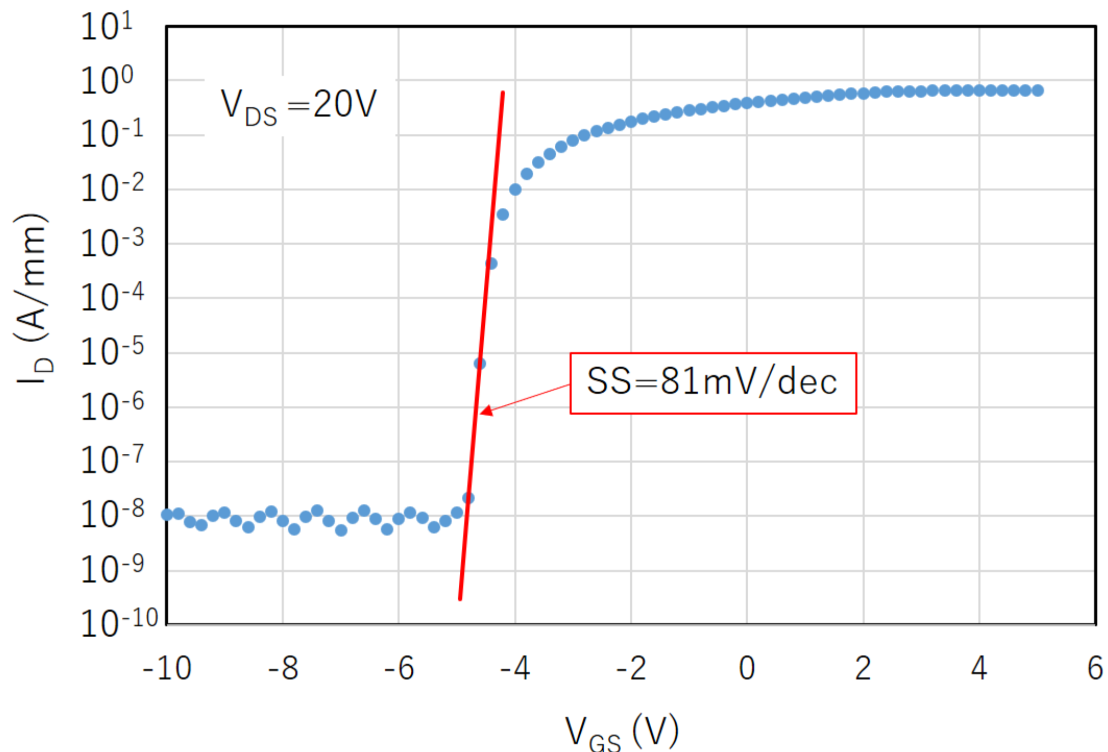

Figure 1. Example of MIS-HEMTs transfer curve and subthreshold swing

To calculate subthreshold swing value from measured data we can simply use the definition of the slope itself: mV/decade. Change in V_{GS} in millivolts required

to change I_D by one order of magnitude.

$$SS_{measured} = 1000 * \frac{V_{GS1} - V_{GS2}}{\log_{10} I_{D1} - \log_{10} I_{D2}} \quad (1)$$

Where $V_{GS1} > V_{GS2}$ and corresponding current values are I_{D1} and I_{D2}. This can be calculated for every pair of points on measured dataset. Since we are interested in the steepest slope, minimal value of SS can be chosen.

Classical expression of Subtheshold Swing for conventional MOSFETs is given by the following equation [2]

$$\mathrm{SS} = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right) \quad (2)$$

where C_{ox}, C_{it} and C_d are capacitances corresponding to oxide layer, interface layer charging/discharging and depletion layer of the semiconductor respectively. *k, T* and *q* are Boltzmann's constant, absolute temperature and unit charge.
When applied directly to AlGaN/GaN MIS-HEMTs, it tends to overestimate the value of SS. In addition to that, SS becomes dependent on the thickness of AlGaN layer [2].
In the paper mentioned above revised equation (3) is proposed, which solves the problem by accounting for AlGaN layer related capacitance C_{AlGaN}. We can also see that C_{it} became $C_{it(dielectric/AlGaN)}$ to specifically point to the interface in question.

$$\mathrm{SS} = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{C_d + C_{it(dielectric/AlGaN)}}{C_{ox}} + \frac{C_d}{C_{AlGaN}}\right) \quad (3)$$

From this equation we can simply derive the value of $C_{it(dielectric/AlGaN)}$

$$C_{it(dielectric/AlGaN)} = \left(\frac{SS * q}{(ln10)kT} - \frac{C_d}{C_{AlGaN}} - 1\right) C_{ox} - C_d \quad (4)$$

For the case of AlGaN/GaN MIS-HEMTs, where un-doped insulating GaN layer is used, only negligible amount of charge resides in the bulk. Therefore, C_d is essentially zero. So simplified equation (5) can be used.

$$C_{it(dielectric/AlGaN)} = \left(\frac{SS * q}{(ln10)kT} - 1\right) C_{ox} \quad (5)$$

Since we use capacitance per unit area in the formula above, D_{it} calculation is extremely simple:

$$D_{it} = C_{it(dielectric/AlGaN)}/q = \left(\frac{SS}{(ln10)kT} - \frac{1}{q}\right) C_{ox} \quad (6)$$

We can see advantages and disadvantages of the method by examining this

equation. Since D_{it} is calculated from $C_{it(dielectric/AlGaN)}$ change near threshold voltage, only the interface states responsive to gate sweep are counted. In other word we only measure a part of total D_{it}, created by shallow traps close to the conduction band.

Advantages of such an approach are simplicity and speed of analysis. No requirement for special devices to be manufactured allows for broad use even in production environment, specifically when comparing different batches of similar devices between each other.

Time domain dynamic resistance analysis

The second method is time domain dynamic resistance analysis. This method for trap level evaluation relies on dynamic resistance measurement data, simplified measurement setup for which is depicted on Figure 2.

Measurement process involves applying stress (V_{ds_off}) to the transistor (V_{DS}) in OFF state ($V_{GS}<V_{TH}$), after which transistor is turned ON and output current (I_D) is monitored.

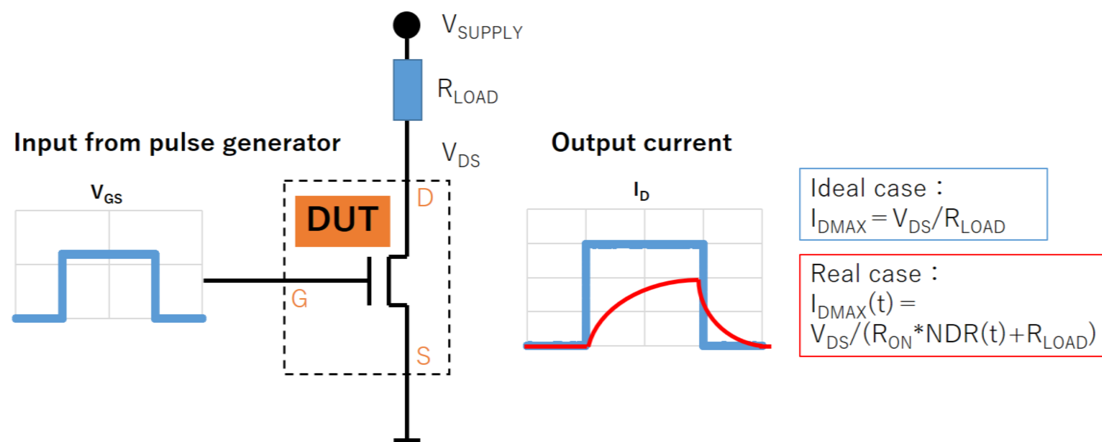

Figure 2. Schematic depiction of current collapse measurement

As depicted on the figure above, In the ideal case I_D would rise instantly and be limited only by load resistance R_{LOAD}. However, in reality, even when channel resistance itself is negligible, dynamic ON resistance must be accounted for as follows:

$$I_{DMAX} = \frac{V_{DS}}{R_{ON}*NDR(t)+R_{LOAD}} \quad (7)$$

So from measured data and equation (7) we can plot dynamic ON resistance

(NDR) against time on logarithmic scale.

We also know, that the release time of trapped electrons is governed by Shockley-Read-Hall [4] statistics and depends of the trap state energy. NDR itself is a combination of traps of multiple energy levels and can be represented using decay time constants τ as follows:

$$\mathrm{NDR} = 1 + \sum_{i=1}^{n} \alpha_i * \exp(-\frac{t}{\tau_i}) \quad (8)$$

Equation (8) is the central piece of this analysis [5,6,7]. We can use it to calculate multiple time constants τ using measured data and fitting. Example of the fitting result is shown on Figure 3.

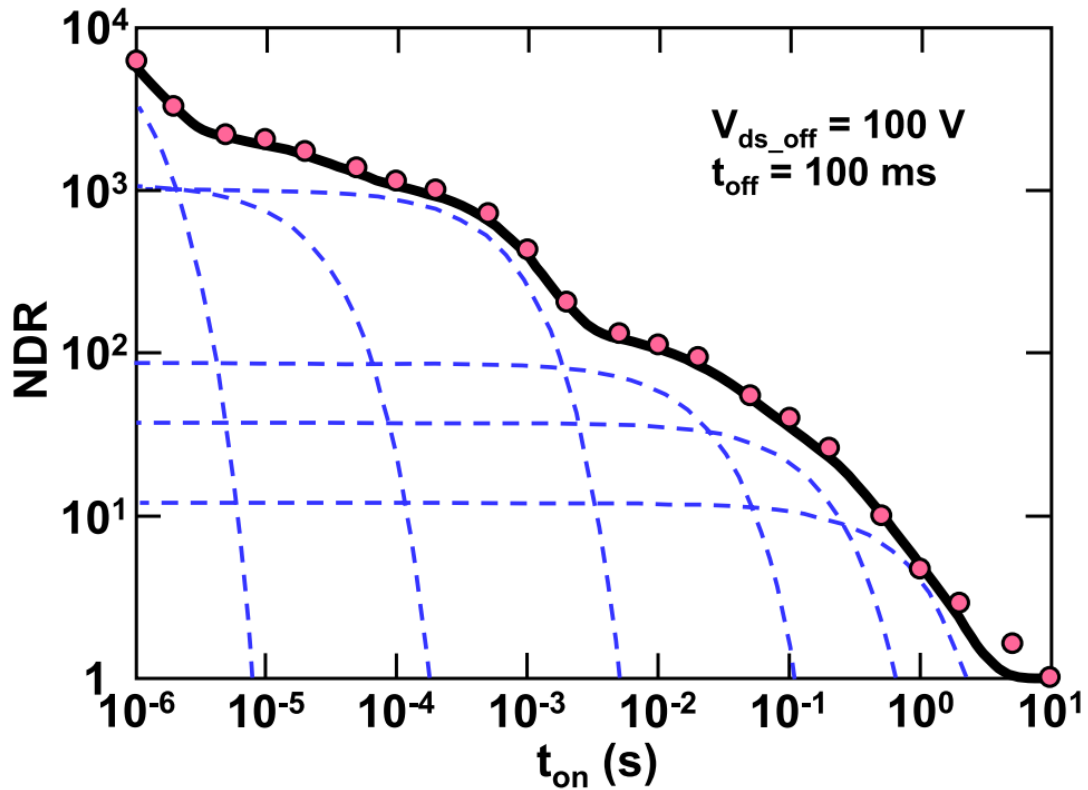

Figure 3. Logarithmic plot of NDR against time. Dots represent measured data, dashed lines represent decay of traps of certain energies. Solid line is a sum of dashed lines [5].

From fitting above we will extract pairs of values τ_i and α_i, where τ_i is a time constant and α_i is a fractional contribution of ith trap level proportional to

corresponding trap density.

To extract trap energy from obtained values we can once again utilize SRH statistics, which links trap lifetime to its energy as follows [3]:

$$\tau_i = \frac{1}{\upsilon_{th}\sigma_n N_C}\exp(\frac{E_C - E_t}{kT}) \quad (9)$$

where υ_{th} is electrons thermal velocity, σ_n is capture cross section of the trap and N_C is the effective state density on the edge of conduction band.

Results of the computations above is given in Table 1, corresponding measured data is plotted on Figure 3.

α_i	τ_i (s)	$E_C - E_t$ (eV)
4968	5.66×10^{-7}	0.27
269	1.80×10^{-5}	0.36
294	2.68×10^{-3}	0.49
142	3.95×10^{-2}	0.56
24	3.97×10^{-1}	0.62
3.6	2.72×10^{0}	0.67

Table 1. Trap analysis result for the example NDR curve [5].

In the essence, this method is a more elaborate version of subthreshold curve analysis, discussed previously in this chapter. Compared to SS based method, transient analysis requires even less device specific data like oxide and AlGaN capacitances while being almost as fast. Data acquired by such analysis is also more graduated – we get exact energy levels of existing traps and can make correlations with their physical origins as was attempted in previous works [8,9]. Method can be further expanded to include temperature of the device [10], as thermal velocity is incorporated in the Equation (9).

However, requirements for measurement setup increase, as we need fast and sensitive current/voltage monitoring, signal generator and signal paths with high rise times as well as fitting software. Main disadvantage is also shared with previous method – we can only discover relatively shallow traps near conduction band, which are responsive to gate sweep. In addition to that, only fractional quantity of total D_{it} is calculated during fitting process. To estimate actual density

of traps

Capacitance-Voltage curve based methods

Third method utilizes capacitance-voltage characteristics of MIS-capacitor. Structure of the capacitor is shown on Figure 4. Outer ring is an ohmic contact, connected to 2DEG inside the substrate. Electrode in the center is separated from AlGaN layer with gate oxide and considered “gate” electrode.

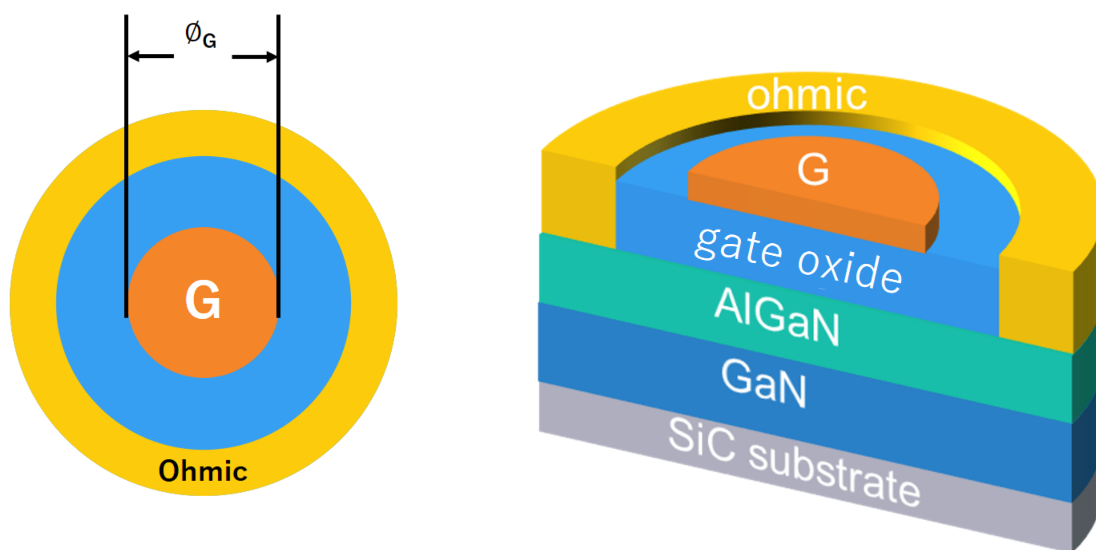

Figure 4. MIS capacitor structure. View from above on the left, cross-section of the epitaxial structure on the right.

Measuring this type of device requires Continuous Wave Capacitance Voltage (CWCV) [11] or Quasi-Static Capacitance Voltage (QSCV) [12] capable measurement setup. Principle difference being that CWCV measurement setup applies continuous sine wave to the Device Under Test to measure impedance and derive capacitance, while Quasi Static Capacitance Voltage Measurement relies on step pulse transient current to determine capacitance by measuring charge. The Gate to Ohmic bias voltage is swept and with each step capacitance is measured to derive the capacitance-voltage curve like on Figure 5. It clearly shows threshold voltage slope and V_{th} value, as well as spill-over phenomenon on the right - the second rising slope on the graph.

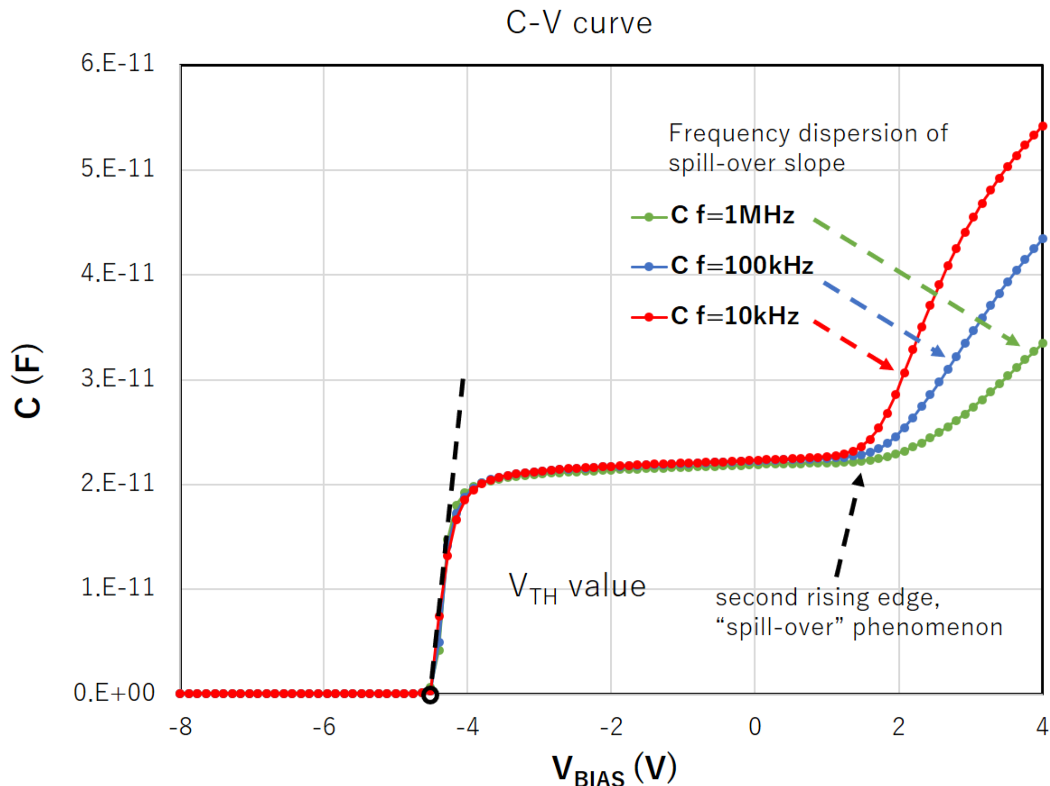

Figure 5. Example CV profile of MIS capacitor

Frequency dispersion method

There are couple of methods of analyzing C-V curves and the frequency dispersion method can be utilized when the spillover slope of the curve is visible and at least two different measurement frequencies are available in the setup. As we can see at the Figure 5, when the measurement frequency is changed the slope of the spill-over clearly changes. We can also define on-set voltage of the spillover by intersecting the linear approximation of the slope with capacitor plateau value and verify that it changes with frequency.

Since we know the frequency, we can calculate the energies of the traps which will respond to them in time with Shockley-Read-Hall model [4], as we did during dynamic R_{ON} transient analysis.

Trap energy would look as follows when computed from frequency instead of time constant [11,14]:

$$E = kT * \ln\left(\frac{\sigma N_C v}{2\pi f}\right) \quad (10)$$

In physical sense it would represent the energy of the trap level, which will be dependent on measurement frequency. Since time constant is inversely proportional to the frequency we will see less traps with its increase.

Area under D_{it} graph from E to E_V can indeed be calculated directly, but it is much more precise to use the difference of two frequencies as follows:

$$\Delta E = E_1 - E_2 = kT * \ln\left(\frac{f_1}{f_2}\right) \quad (11)$$

And the calculation of the D_{it} between energy levels 1 and 2 is greatly simplified:

$$D_{IT}(E = E_{AVG}) = \frac{C_{Insulator}}{q} * \frac{\Delta V}{\Delta E} \quad (12)$$

Where $E_{AVG}=E_1+\frac{\Delta E}{2}$, an average value between E_1 and E_2. As we can see when using two frequencies we do not need to assume the value of capture area σ, making the calculation even simpler.

In conclusion – this a simple and reliable method for calculating state densities in the vicinity of conduction band. Since high frequency CV analysis equipment is affordable this can be used to directly measure multiple points on the acceptor like region of D_{it}.

At the same time disadvantages are the need for special device structure to be fabricated and the possibility of device breaking down from positive bias before spill-over slope can be visible. It somewhat limits this technique to devices with better interface characteristics [15,16].

C-V curve fitting method

In comparison to previous methods the calculation of D_{it} from single C-V curve is not that straightforward, requiring us to solve one dimensional Poisson equation for electric potential profile and apply numerical methods for fitting. The groundwork in laying out the method utilized in D_{it} calculation for MIS-HEMTs was performed by M. Miczek et al [13] in 2008. Here I will describe the simplified flow of derivation performed in the paper above. Their group has created a generalized one dimensional model of the AlGaN/GaN based MIS capacitor and composed a Poisson equation (10) based on it.

$$\frac{d^2V}{dx^2} = -\frac{q}{\varepsilon_S\varepsilon_0}(N_D - n + p) \quad (13)$$

Where V(x) is a one dimensional electric potential, $\varepsilon_S\varepsilon_0$ is semiconductors

dielectric constant multiplied by vacuum permittivity, N_D, n and p are concentrations of ionized dopants, electrons and holes. q is the elementary charge.
Next, the boundary conditions were given:

in the insulator $\frac{d^2V}{dx^2} = 0$

at the gate (x=0), $\mathrm{V} = V_G - \frac{\phi_s}{q} + \frac{\phi_b}{q}$

where ϕ_s and ϕ_b are surface barrier height and built in potential in energy units. Finally, Neumann boundary condition was used to describe insulator-semiconductor interface, $\varepsilon_S\varepsilon_0 F_S - \varepsilon_I\varepsilon_0 F_I = Q_{IT} - Q_{FIX}$
where F is an electric field density and is equal to -dV/dx, for semiconductor (S) and insulator (I). Q_{IT} and Q_{FIX} are interface trap and fixed charge sheet densities respectively.

To further constrain the Poisson equation above two other equations were derived. M. Miczek et al assumed two types of D_{IT} distributions in the work: Gallium (acceptor-like) and Nitrogen (donor-like) specific Gaussian curve peaks (11) as well as more general disorder-induced gap state U-shaped (12) D_{IT} model.

$$D_{it}^{A,D}(E) = D_{it\ max} exp\left[-4log2\left(\frac{E-E_{A,D}}{FWHM}\right)^2\right] \quad (14)$$

$$D_{it}^{A,D}(E) = D_{it0} exp\left[\left(\frac{|E-E_{CNL}|}{E_{0A,0D}}\right)^{n_{A,D}}\right] \quad (15)$$

Finally, fixed interface charge density Q_{FIX} was calculated from polarization charge of AlGaN/GaN interface using lattice and piezoelectric constants as follows:

$$Q_{fix}(AlGaN/GaN) = |P_{pe}(AlGaN/GaN) + P_{sp}(AlGaN/GaN)|$$

where P_{pe} and P_{sp} are piezoelectric and spontaneous charges in AlGaN/GaN interface.

The theoretical value of $Q_{fix}(AlGaN/GaN) = 1.2\mathrm{x}1013\ \mathrm{q/cm^2}$ for $Al_{0.25}Ga_{0.75}N$/GaN was overestimating the value measured experimentally by other groups, so they adjusted it to $9\mathrm{x}10^{12}$ q/cm^2 match the threshold voltage of measured device.

As final step the numerical fitting was performed by specialized differential equation solver software to receive the whole D_{it} curve as seen on Figure 7.

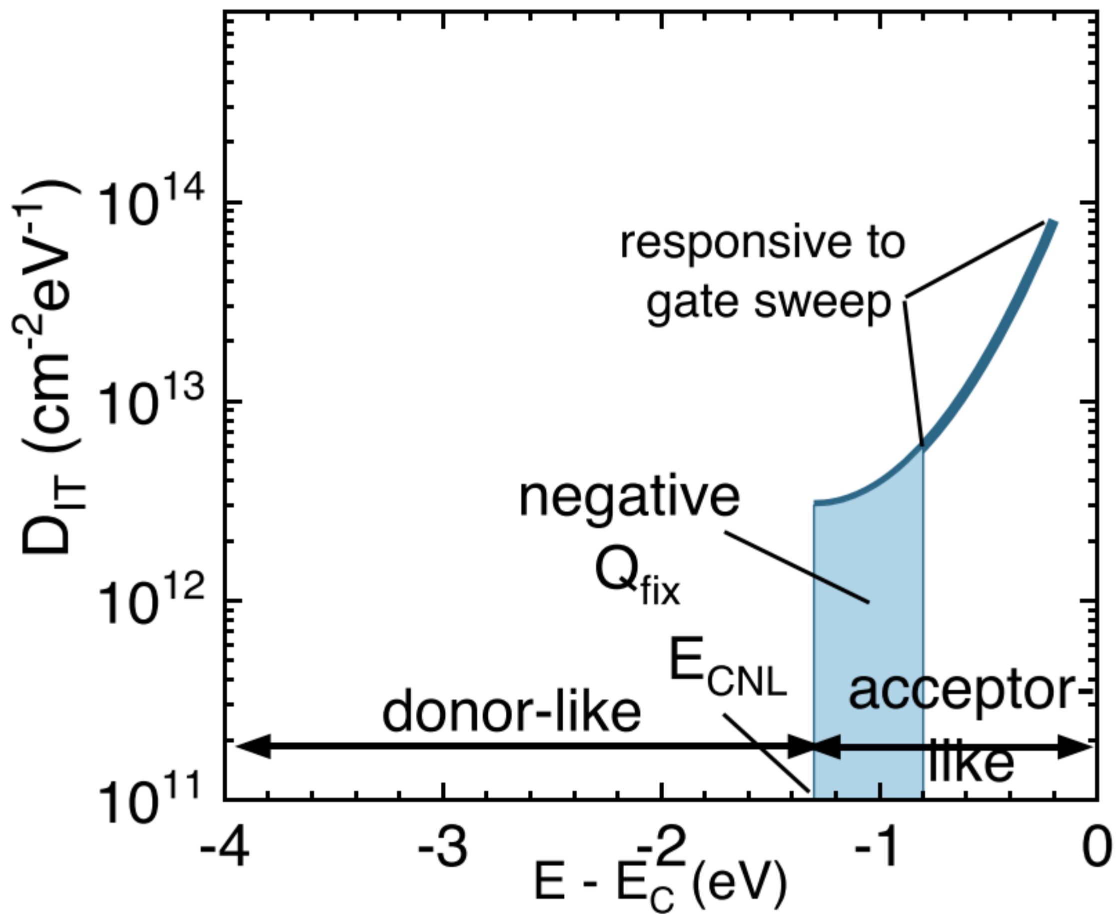

Figure 6. Example result of D_{it} derivation [14]

In summary, this method is by far the most computationally intensive, it requires specific software and a set of conditions for it to work. For example, if in the measured C-V curve spill-over is not visible the number of possible solutions becomes infinite. To resolve this, more points need to be somehow measured on the D_{it} curve. Usually it is achieved with methods described in this chapter.

On the other hand, this is an incredibly powerful tool to link different measurement methods and perform cross verification, even when they measure at different trap energies. In conclusion, this tool provides best accuracy when used with other measuring techniques to constrain the fitting algorithm.

Photo-assisted threshold voltage shift measurement

Previously discussed methods monitor acceptor-like traps responsive to gate sweep and one way or another utilize SRH statistics for D_{IT} calculations. Photo-assisted threshold voltage shift measurements however, do not. Core of the method is to pre-stress the device to fill all trap levels possible and selectively de-trap energy levels with monochromatic light. Difference can be measured by observing the shift in threshold voltage. The technique and necessary derivations were presented in a number of papers [16,17].

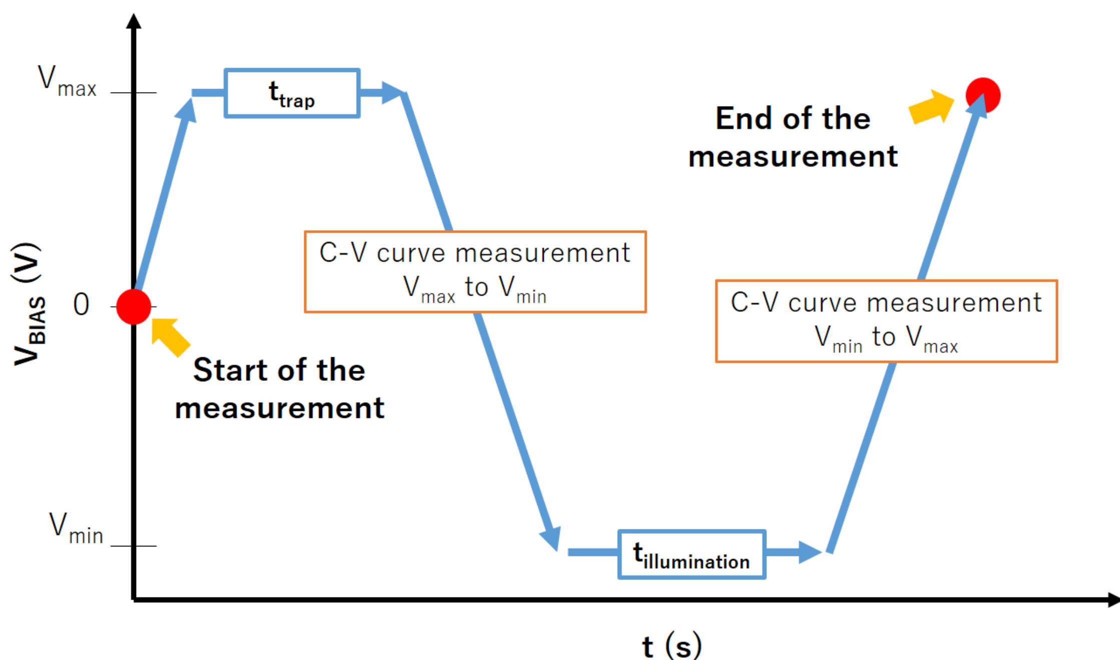

Figure 7. Timeline of Photo-assisted C-V measurement

MIS capacitor is used for this measurement and the corresponding structure was depicted on Figure 4. The timeline of the measurement is depicted on Figure 7. Horizontal axis is time of measurement starting from zero, vertical axis represents gate-source voltage V_{GS}. Whole measurement relies on careful control of the illumination, so the testing setup must be shielded from light. First we start at V_{GS} = 0 V and sweep it to V_{MAX}, which is above 0 V. This is done to avoid elevated transient currents, which can damage the MIS capacitor. Then with bias voltage turned ON we wait for t_{trap} to fill all trap energy levels with electrons. The next step is to sweep towards negative voltage, which is lower than V_{th} of the device while measuring the capacitance. Then we illuminate the device for time $t_{illumination}$ with

known wavelength of monochromatic light. This must vacate all traps with energies lower than the energy of applied light. Finally, the light is turned OFF and negative to positive voltage sweep with C-V curve measurement is performed.

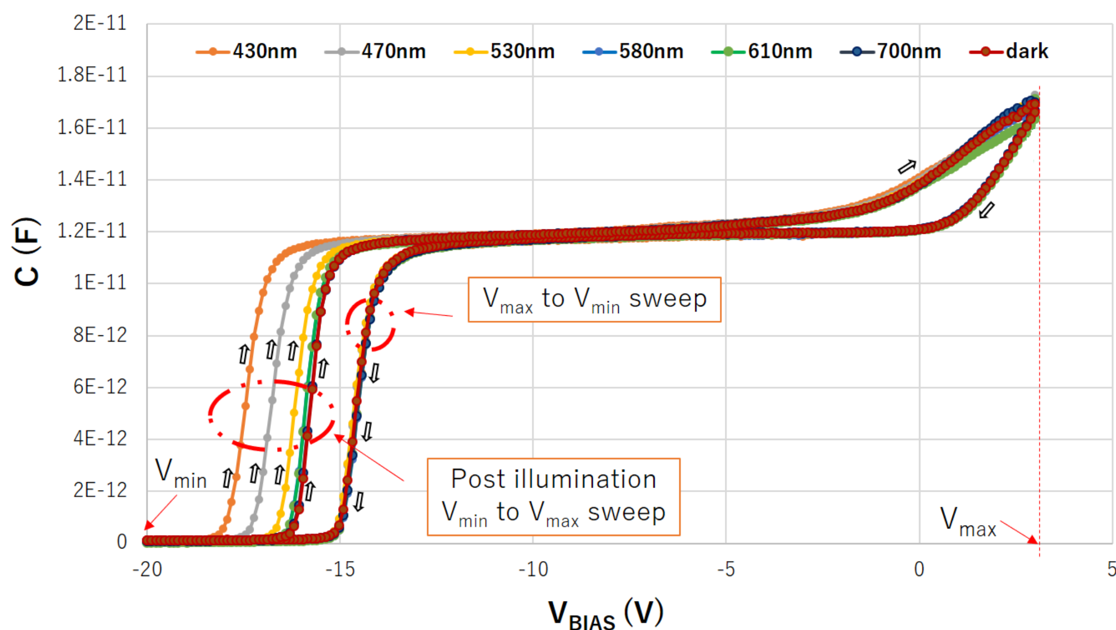

Figure 8. Example of measured curves.

On Figure 8 we can see a number of overlapped C-V curves. With the decrease in wavelength of light we see gradual shift of threshold voltage in negative direction. At higher wavelengths this does not happen and becomes equal to the natural hysteresis of the device labeled "dark", as it was measured without illumination. This type of hysteresis is likely due to shallow traps, which have enough time to de-trap during voltage sweep and we do not use it in the analysis directly. We can also see that downward slopes of all curves essentially overlap, which indicates that traps fill to the same extent when the stress is applied.

This brings us to an important part of this measurement – the choice of times t_{trap} and $t_{illumination}$. They must be tweaked as follows to ensure correct results:

1. First we set arbitrary values to both parameters and perform the measurement.
2. Second measurement is performed with doubled illumination time, but the same wavelength.
3. Upward slope of both runs is compared and if there is a difference in threshold voltage - $t_{illumination}$ is increased again and measurement is repeated until there is no change.

This assures that all available traps are vacated. Real time depends on light source intensity and position.

After the illumination time was set, downward slopes of consecutive measurements get compared across multiple consecutive measurements and wavelengths. This ensures that stress time is enough to fill all available trap levels. Finally, $t_{illumination}$ adjustment is performed once again to ensure trapping and de-trapping saturation.

Derivation of D_{IT} itself was already described in Equation (12), but this time the difference in energy is calculated as follows:

$$\Delta E = \Delta h\nu = h(\nu_1 - \nu_2) \quad (16)$$

where *h* is a Plank's constant.

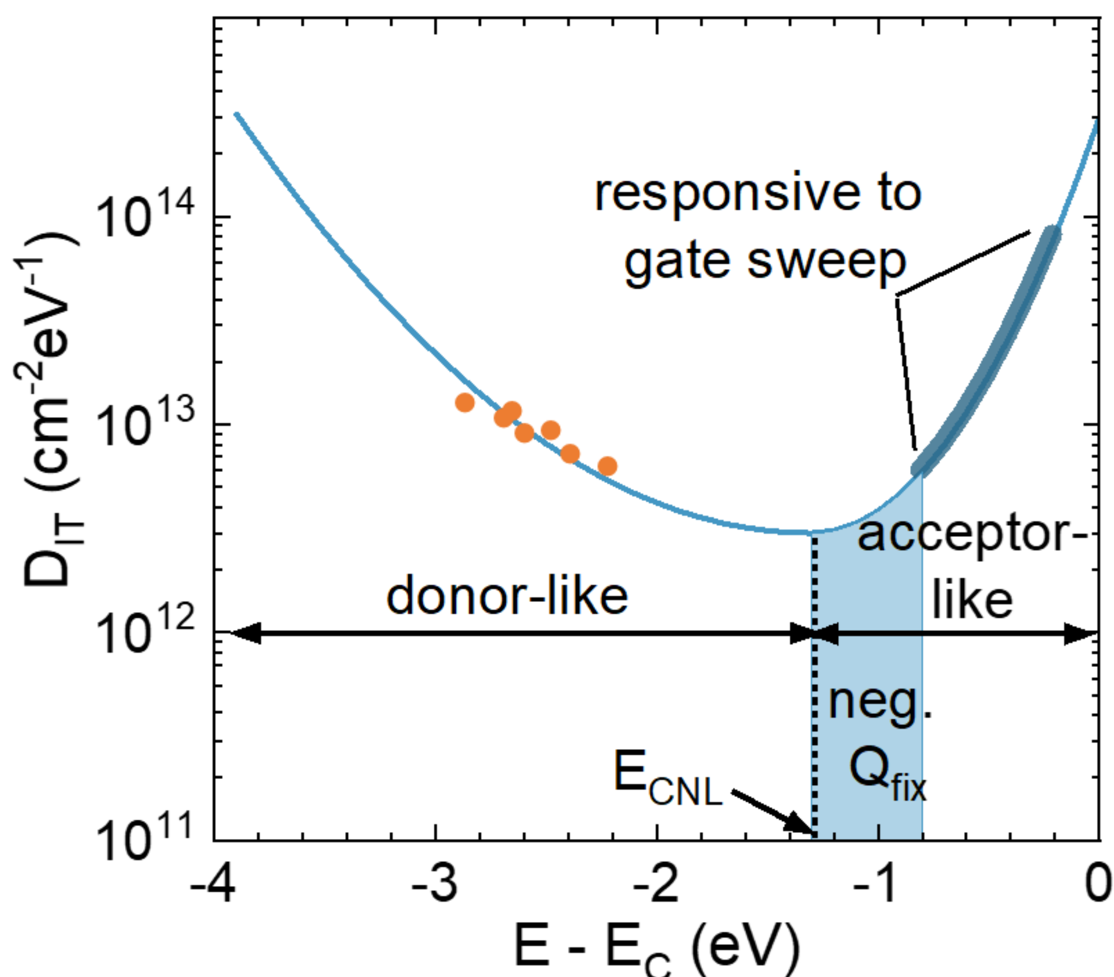

Figure 9. Photo-assisted D_{it} derivation result.

On Figure 9 we can observe how points measured with Photo-assisted C-V

method (orange dots) are overlapping with D_{it} curve obtained with numerical fitting (thin blue line). We can also see thick blue line, which highlights the region of the curve, measurable with gate sweep methods alone.

Summarizing, this method's strong sides are the extremely high flexibility in choice of energy level to be measured and it's the unique ability to measure and differentiate between high energy trap levels.
Negative sides expand the list of ordinary C-V measurements like specific device structures and complexity in measurement setups with variable wavelength monochromatic light source and the need of the dark enclosure. Finally, measurement times make it an extremely long and laborious process, hardly suited for production environment.

In this research we used these methods in different combinations to save time while assessing as much devices as possible.

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Chapter 3 AlGaN/GaN-HEMT production process

Production process utilized in this work uses commercially available AlGaN/GaN epitaxial wafers on semi-insulating SiC substrate. Structure and photo of the wafer depicted on Figure 1.

Figure 1. Structure of the wafer (left) and its packaging (right)

Wafer dicing and pretreatment

During small-scale research and development using the whole wafer a once usually is not optimal. With many parameters to optimize and small amount of samples to be measured per batch more sensible approach is to dice the wafer into smaller pieces and use them separately.

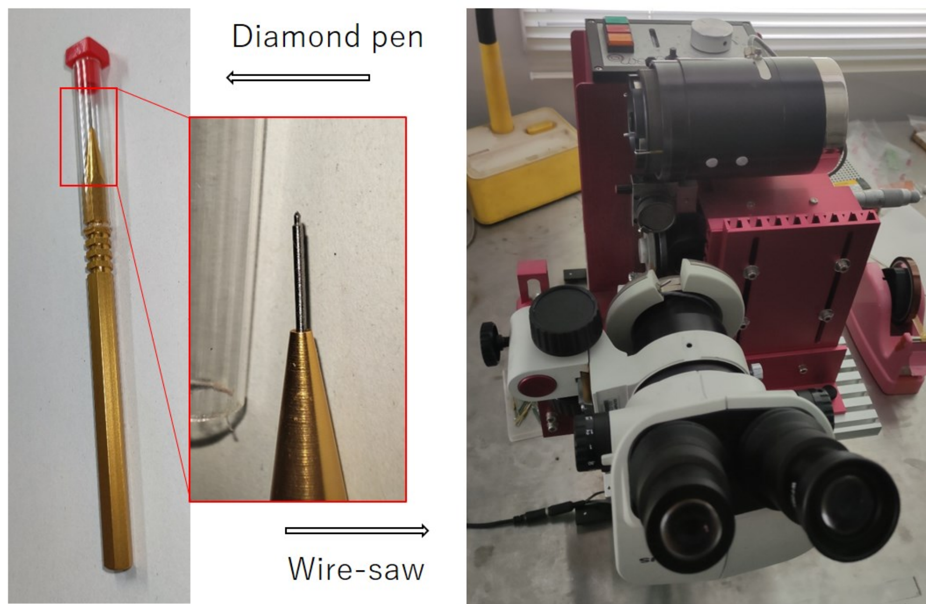


Figure 2. Options for wafer cutting

Depending on required accuracy and size, tools on Figure 2 can be used: precision diamond pen on the left or diamond wire-saw on the right.

During handling and cutting AlGaN surface has to be protected from contaminations and physical damage. Many ways of protection exist, but in this work we opted for photoresist coating. We do use the same coating further in the process, so it saves us from handling another set of chemicals.

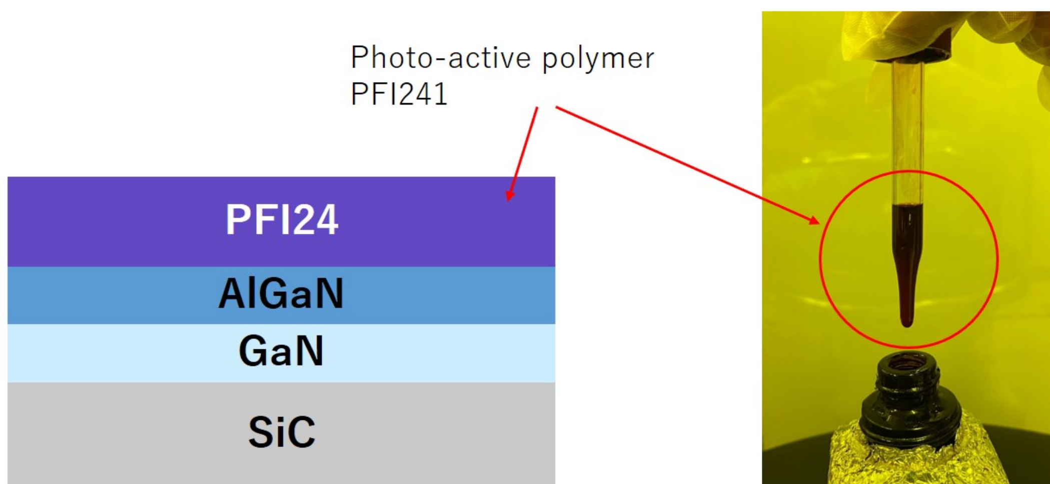


Figure 3. Protective coating before cutting.

As depicted on the figure above, PFI241 was used. To apply it evenly to the whole surface it was spin-coated for 60 seconds at 3000 rpm and baked at

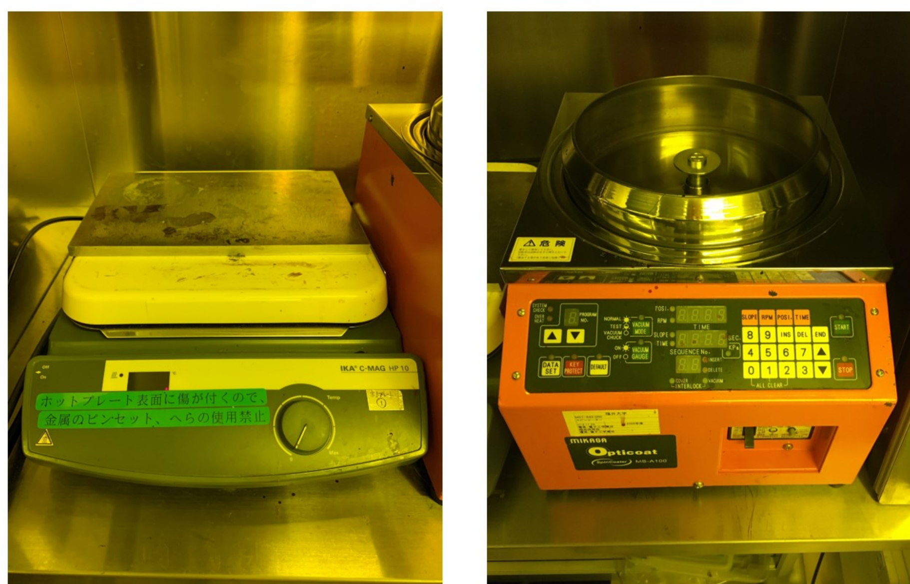


Figure 4. Hot plate [IKA C-MAG HP10] (left) and Spin-coater [Mikasa Opticoat Spincoater MS-A100] (right)

110℃ for 60 seconds to completely harden the photoresist. After that, wafer might be cut into smaller samples. Depending on the state of the wafer (single-side polished double side polished) it might be necessary to mark the reverse side of the sample to avoid confusion during handling.

After that, samples must be ultrasonically washed with pure acetone, pure ethanol and rinsed in de-ionized water for at least 5 minutes for each step. This step will be used multiple times afterwards, so I will call it organic solvent treatment for brevity.

Samples that have been stored for prolonged amounts of time should be washed with Buffered Hydro Fluoric acid to remove natural oxides and surface contamination. AlGaN layer does not react with BHF at room temperature, so 5-minute-long cleaning was performed.

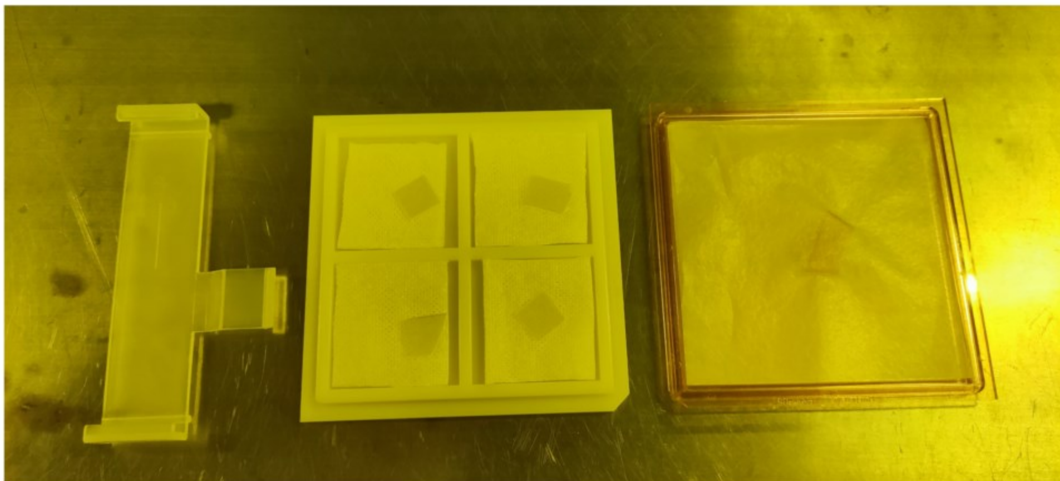


Figure 5. Diced samples in shock absorbing holder.

Device isolation

Device isolation or mesa etching was performed with Inductively Coupled Plasma – Reactive Ion Etching (ICP-RIE). This process is anisotropic, meaning accelerated ions have a direction, along which etching speed is maximal and perpendicular to that – low enough to be neglected.

To perform photolithography on the samples we again have to apply photoresist, as described on Figure 3. However this time baking temperature is 90℃ for 60 seconds, so photoresist does not harden completely and still responsive to UV light. After that, samples are set into contact photolithography aligner and mask made of UV-transparent glass with metal patterning pressed against the surface

of the sample. After exposure was finished, post-baking step is performed on a hot-plate (110℃ for 60 seconds).

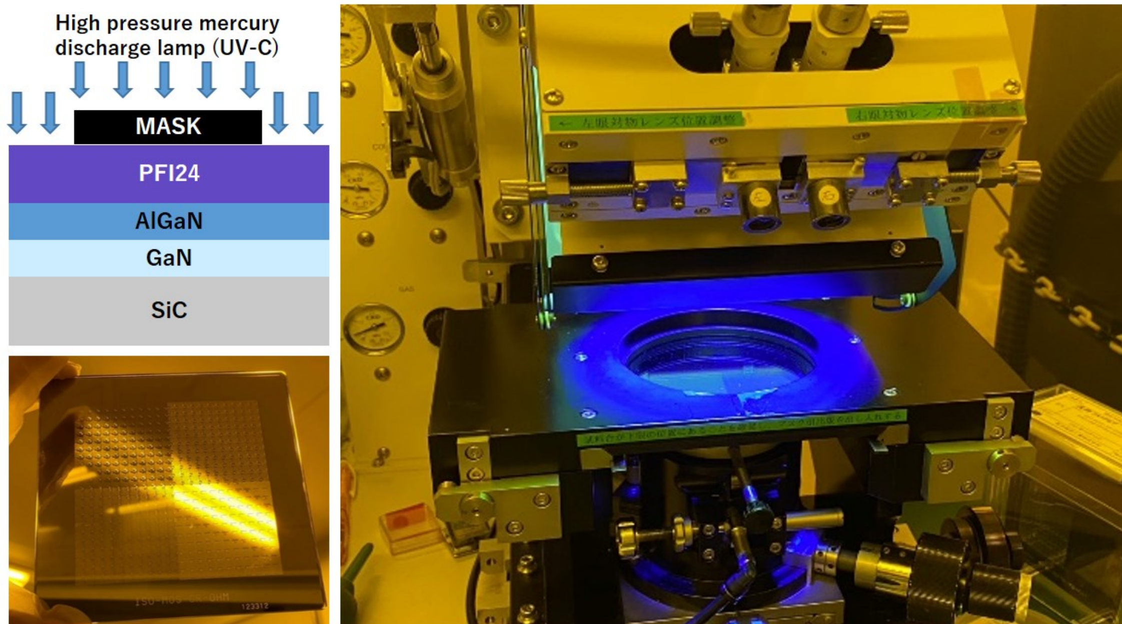


Figure 6. Contact photolithography process. Top left- simplified cross section, bottom left – semi-transparent photo-mask, right – mask aligner during exposure [Mikasa Presicion Pattern Mask Aligner MA-20AC].

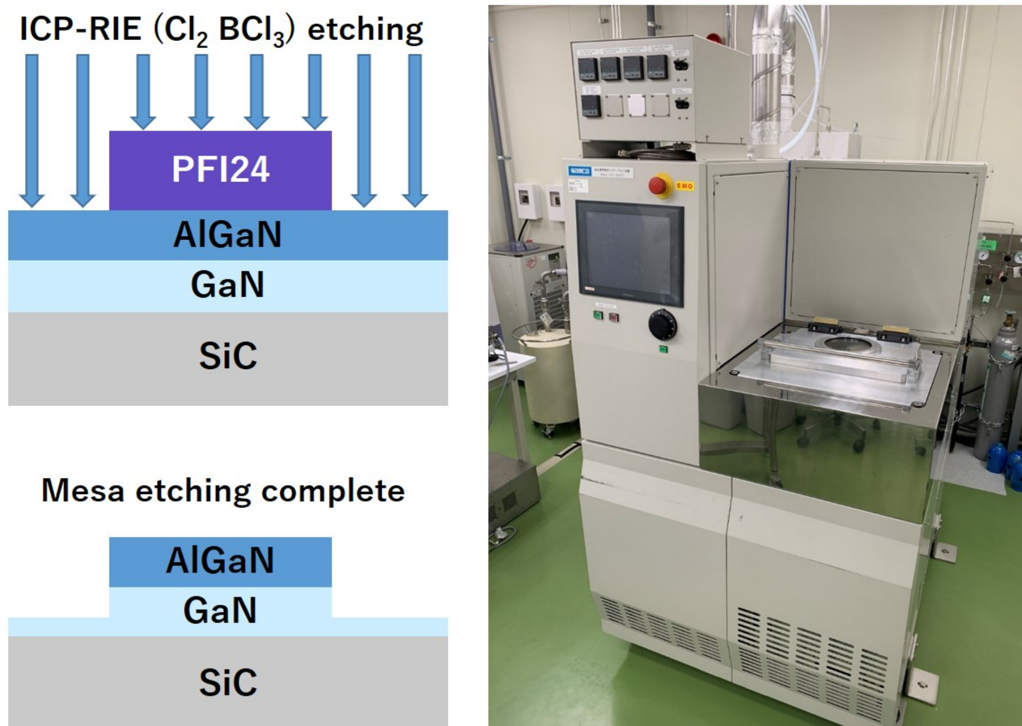
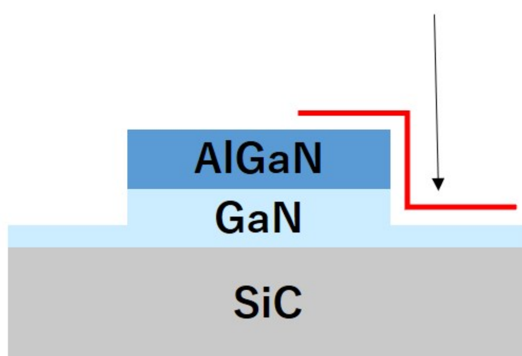


Figure 7. ICP-RIE process [SAMCO RIE-200iP].

After that, portions of polymer (PFI241) that were exposed to light become soluble in the developer solution. After manual rinsing in developer liquid (NMD-3) and washing with deionized water samples are loaded into ICP-RIE machine and mesa etching is performed as can be seen on Figure 7. Conventional for AlGaN/GaN etching gases are Cl_2 and BCl_3 were used. After etching, leftover photoresist is removed by organic solvent cleaning and ideally AlGaN layer and some GaN layer is etched away, as on the bottom left of Figure 7. To verify that, two dimensional step profile measurement is performed.



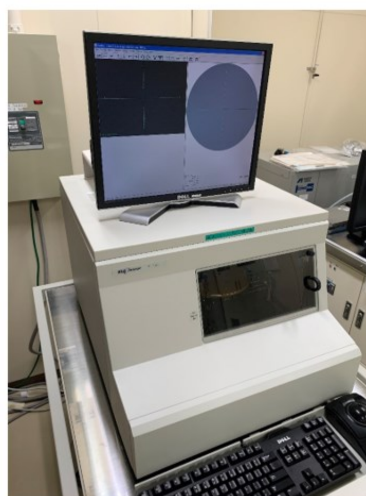


Figure 8. Mesa depth verification [KLA Tencor P-16+]

Ohmic contact formation

Formation of metallic contacts, being an additive process, requires more elaborate photo-active coating. It consists of 3 layers, as depicted on the left side of Figure 9.

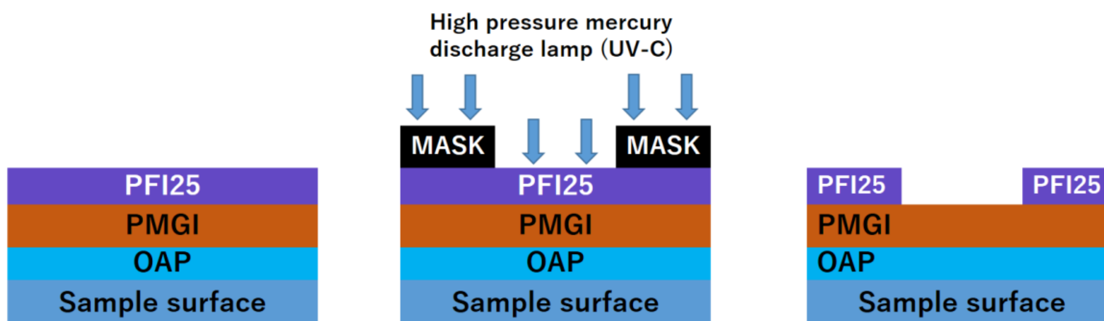


Figure 9. Two-layer photoresist process (undercut layer).

Coating is done by the same spin-coater as explained previously. First layer (OAP) is an adhesion regulating chemical, similar to glue. It is spin-coated for 60 seconds at 3000 rpm and second layer (PMGI) deposited on top of it with the same spinning setting right after. Next, the sample is baked at 200℃ for 60 seconds and PFI25 layer is spin-coated on top (3000rpm, 60s). Final baking step is the same as for PFI241 - 90℃ for 60 seconds.

Exposure process is pretty much the same in the beginning, as depicted in the center of Figure 9. Sample is exposed and the top layer of photoresist is developed with NMD-3 developer.

Next, underlying layers have to be treated separately. First Baking oven is used (Figure 10, left) to completely harden and dry PFI25 layer (120℃, 20 minutes). It makes it non responsive to developing solutions and light.

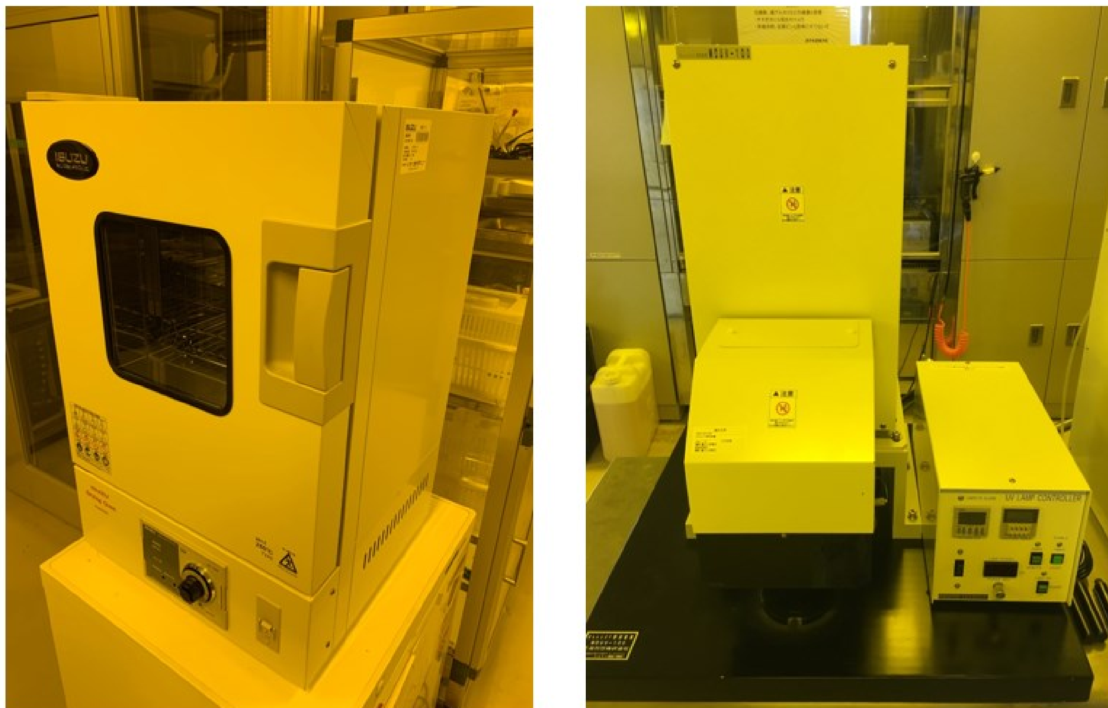


Figure 10. Drying oven [ISUZU ASN-111] (left) and Deep-UV exposure chamber [Mikasa DeepUV MDUV-100] (right)

Next, Deep-UV source is used to completely expose PMGI layer to UV light (500W, 5min). After that samples are baked on 110℃ hot plate for 10 minutes and finally developed with PMGI developer solution.

Cross-section of this photoresist stack can be seen on Figure 11 (left). PMGI and OAP layers develop sideways, undercutting the PFI25 layer, that is why bottom layer is sometimes called an undercut layer. Since additive processes like

metal deposition are not completely anisotropic, some material inevitably covers the sidewalls of the photoresist. If used with single layer photoresists, it would prevent clean separation of the material deposited on the photoresist from material deposited on the surface of the sample.

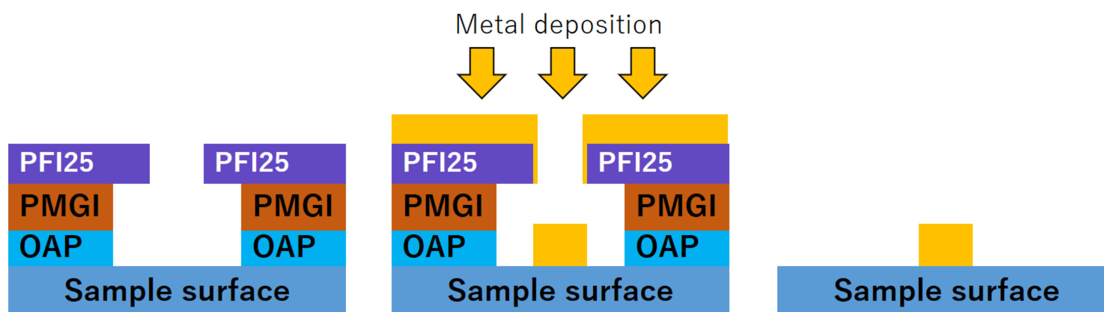


Figure 11. Two-layer photoresist and its use

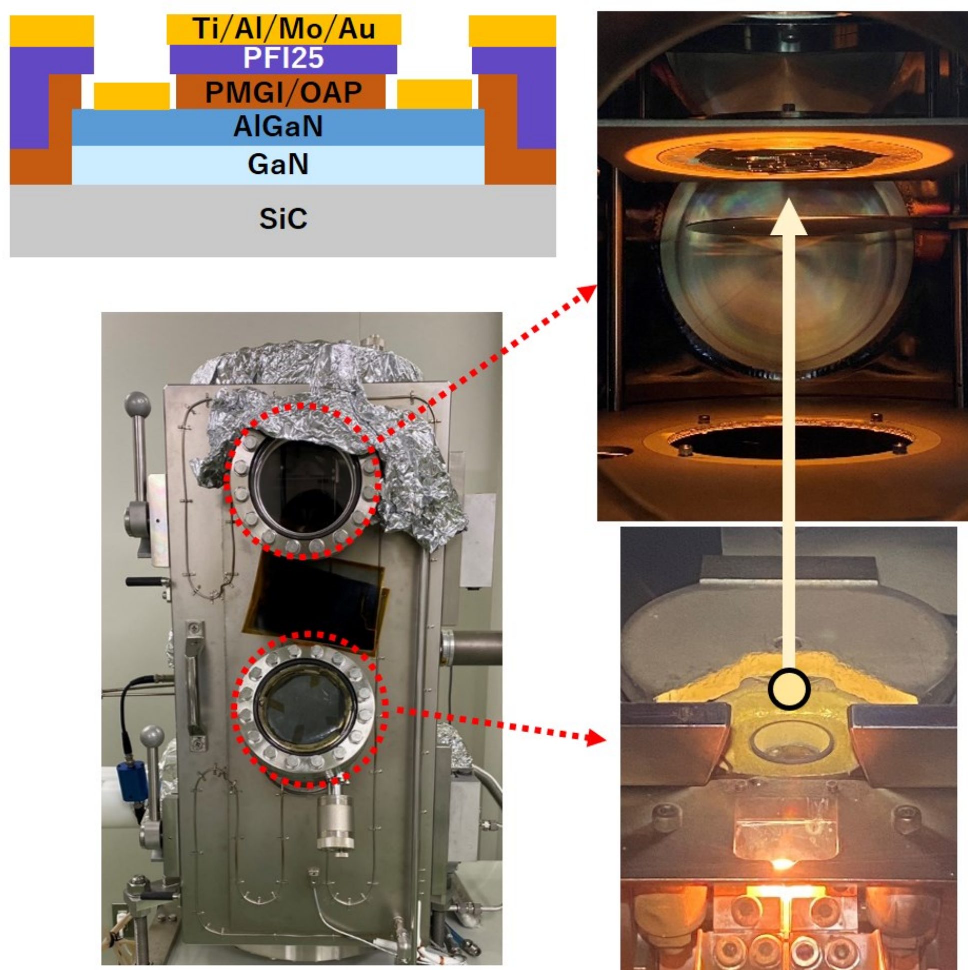


Figure 12. Vacuum EB-PVD setup [Modified Sanyu Electron SVC-700LEB].

Metal deposition itself was carried out in vacuum EB-PVD setup, as depicted on Figure 13. For conventional Ohmic contact to AlGaN Ti/Al/Mo/Au metal stack is used, with the thicknesses of 15/60/35/50nm respectively.

Lift-off is a two-step process. First, PFI25 layer is dissolved in acetone, this makes metal on top of photoresist to flake off. To completely remove it ultrasonic bath is used with subsequent washing with ethanol and deionized water.

Finally, PMGI/OAP specific removal solution is applied in a heated bath (90℃ for 20 minutes) and all the residue is washed off with organic solvent cleaning process. Then, the sample is ready for Rapid Thermal Annealing.

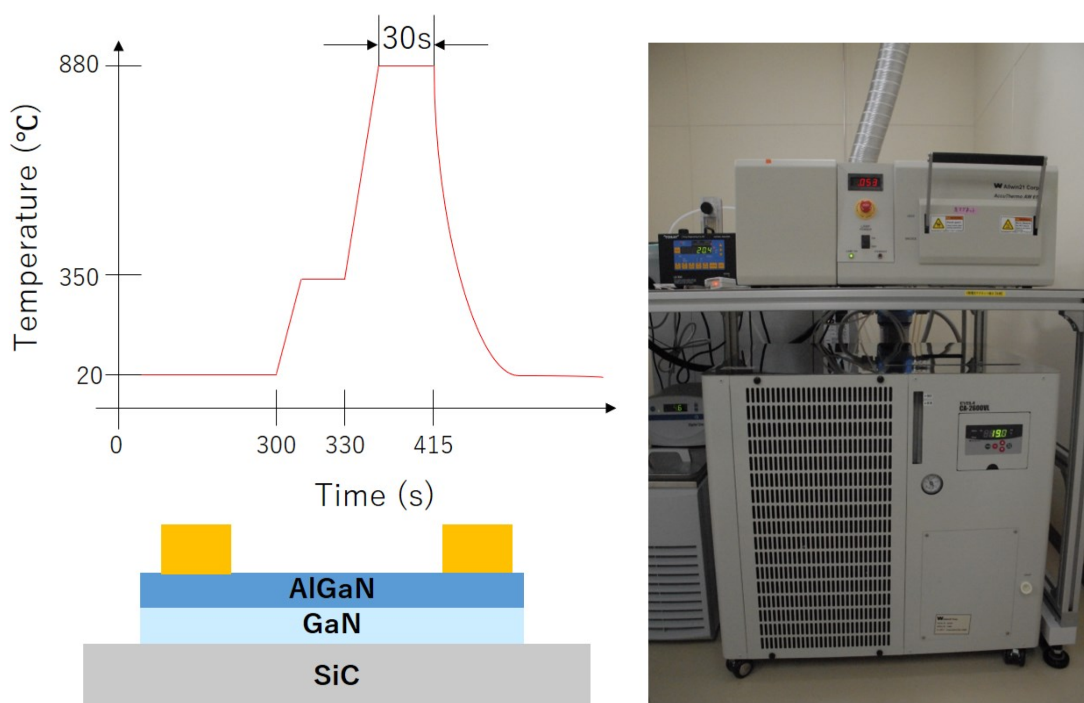


Figure 13. Rapid Thermal Annealing [Allwin21 Corp. AccuThermo AW610]

When Ohmic contact stack is deposited, it is technically still a Schottky contact. For its IV characteristic to become linear and ohmic-like it has to be annealed. On Figure 13, RTA temperature profile is displayed on the top left. First the chamber is purged with pure Nitrogen to prevent oxidation of the sample during annealing. Oxygen content is monitored and kept below 10ppm. After there is a pre-heating step to 350℃ to avoid temperature overshoot later, stabilization time of 30s and fast heating to desired temperature of 880℃. After 30 seconds pass, heaters are turned off and cooling is activated. After TLM measurements need to

be performed to verify contact resistance and linearity.

Gate Insulator and Gate metal deposition

After Ohmic contact has been obtained and measured it is important to clean the surface as best as possible. We have utilized prolonged ultrasonic cleaning in organic solvents (10 minutes each), followed by 30 second BHF dip. After that samples were dried with nitrogen stream and inserted into deposition chamber.
Gate insulator deposition was carried out with thermal Atomic Layer Deposition (ALD). Setup is depicted on the Figure 14, below. With Pure Nitrogen as a carrier gas, Ozone as an oxidizer and Trimethylaluminium (TMA) as a source of Aluminum. Ozone was generated using Ozone generator and pure oxygen supply.

Figure 14. ALD setup [Cambridge NanoTech SavannahS100-4PVP]

Deposition chamber temperature was kept at 250℃ to ensure amorphous oxide layer formation.
After that, devices were washed again in organic solvents, coated with two-layer

photoresist and exposed through the gate mask. Developing, deposition and lift-off process was exactly the same as for ohmic stack. The only difference was the stack itself: 50nm of Nickel and 150nm of gold was used as a gate electrode.

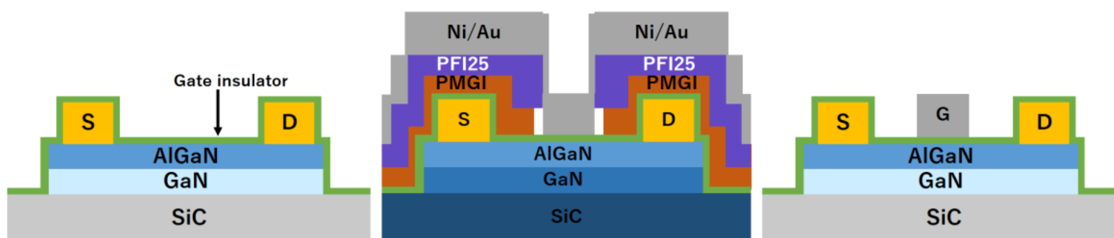


Figure 15. ALD deposition, Gate metal deposition and device after lift-off

Passivation and contact hole etching

At this point in production process devices on the sample would be measurable, given the probe penetrates insulator layer. However, devices must be passivated to protect them from environment. This is done with Argon plasma sputtering, setup for which is depicted below.

Figure 16. RF plasma sputtering setup [TOKUDA CFS-4ES].

In theory, ALD is also usable for passivation, but deposition time for a sufficiently

thick layer would be order of magnitude longer compared to sputtering. As depicted on the left of Figure 17, thick layer of Silicon Nitride was deposited on the device.

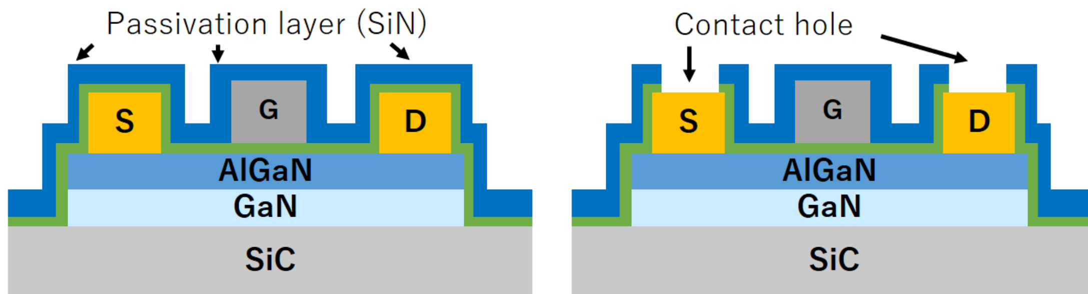


Figure 17. Sputtering result and CH etching.

Etching process for contact holes is similar to mesa etching. First the samples are cleaned with organic solvents, single layer of photoresist is deposited, exposed and developed. Finally, Compact Etcher setup, as on Figure 18 is used for ICP-RIE.

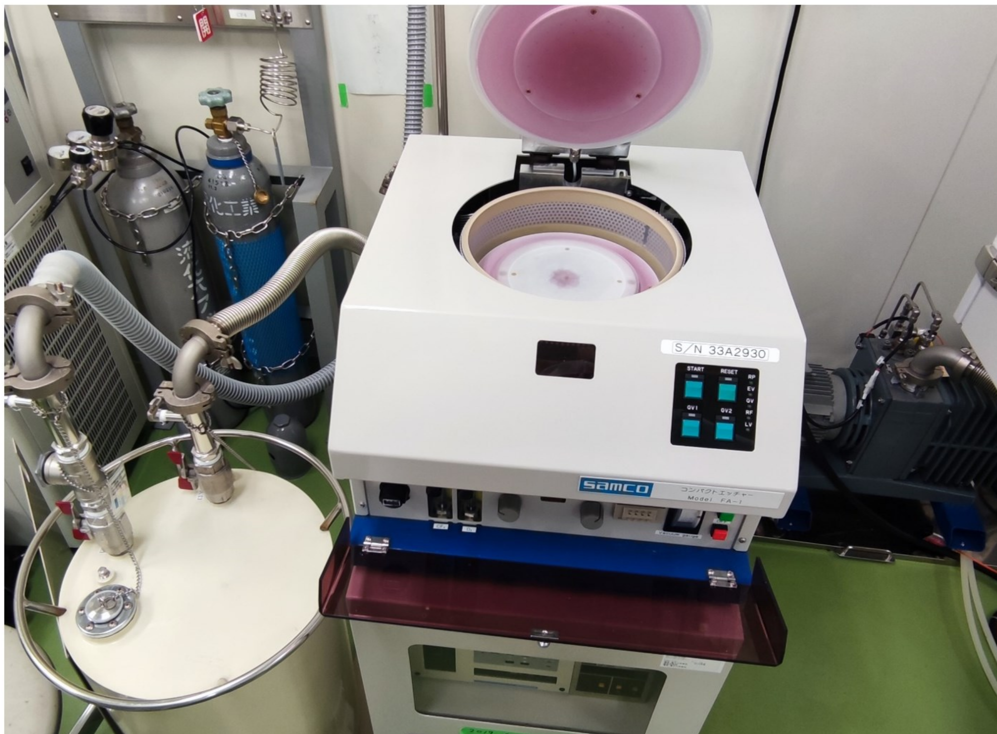


Figure 18. Compact Etcher setup [SAMCO FA-1].

This time, however, CF_4 was used as a process gas. Finalized device cross-

section can be seen on the right side of Figure 17. Gate contact pad was also etched, but is not shown on the cross-section.

In the end of this chapter I would like to address the apparatus that is used continuously throughout the manufacturing but often overlooked in other works. That is Ultra-clean deionized water source, machine depicted on Figure 19. Water is passed through microscopic filter, carbon absorber and multiple ion exchange resin tanks, micro-organism contamination is controlled with UV-C sterilization. Quality of the water is monitored by electric resistance and is checked prior to use to be equal to 18.2 $\mathrm{M\Omega \cdot cm}$.

Figure 19. Deionized water plant [UL-pure with storage tank]

Measurement and evaluation

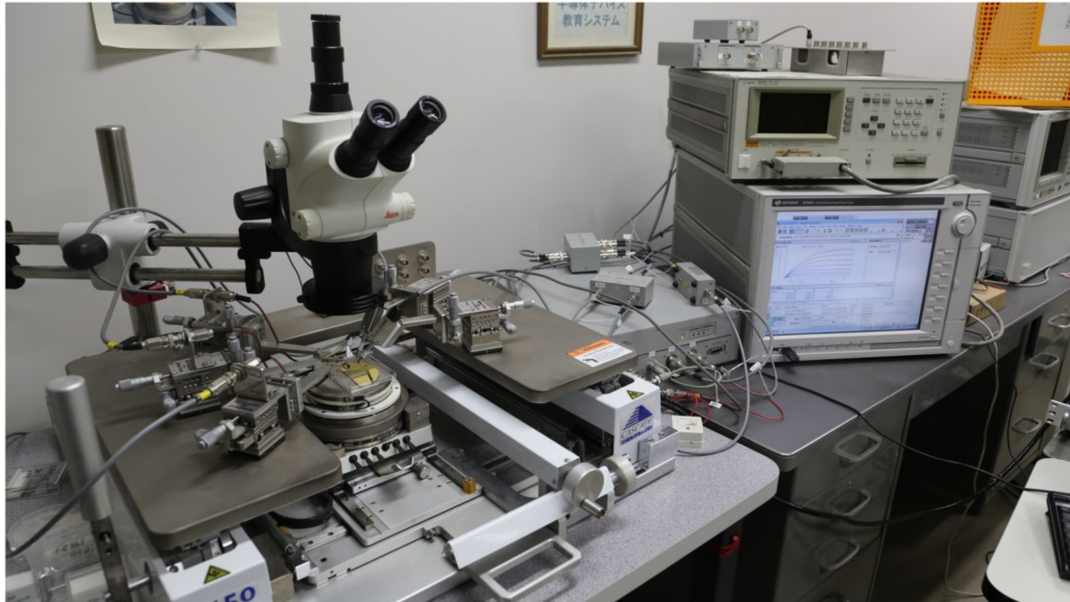


Figure 20. Semiconductor parameter analyzer [Agilent B1505A].

Figure 21. Capacitance-Voltage measurement system [Agilent 4284A].

All DC measurements were performed with Agilent B1505A Semiconductor Parameter Analyzer, as on Figure 20. Kelvin probes were used for Source and Drain electrodes, while Gate was connected with a single lead.
Capacitance Voltage measurements were performed with Agilent 4284A Precision RCL Meter, as on Figure 21. Computer was used for automation and control via GPIB communication port. For Photo-assisted CV measurements, Xenon Light source LAX-C100 was used with a set of monochromatic filters, as depicted on Figure 22. Automation was done by serial communication to C-V measurement system. Pinpoint illumination was realized with optic fiber and a lens system, as on Figure 23.

Figure 22. Monochromatic light source [LAX-C100].

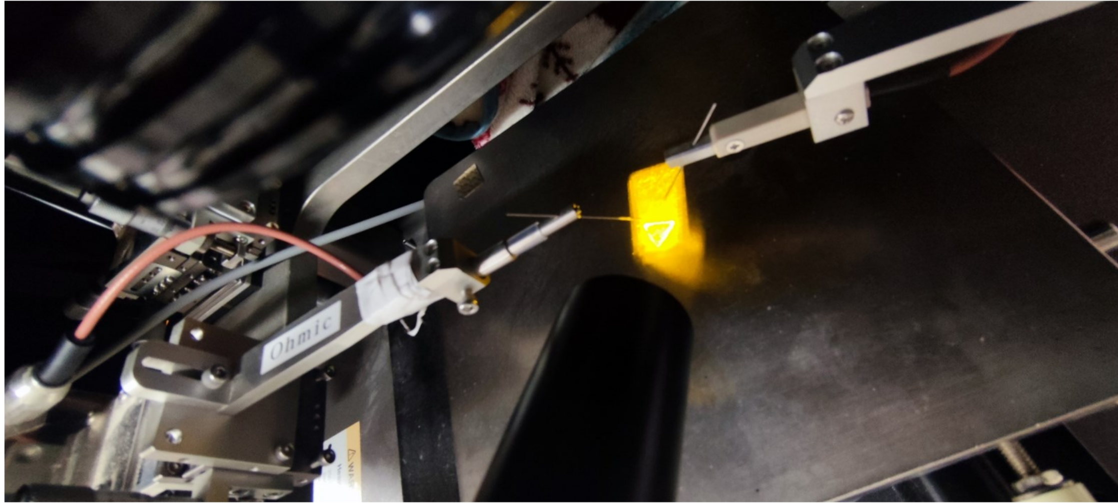


Figure 23. Device illumination with light fiber optics

Chapter 4 D_{it} control methods implemented

As described in Chapter 3, even the simplest device fabrication process includes multiple steps, each of which has potential impact on device performance. In our research we aimed at two processes with the highest temperatures in the entire production flow. These are the epitaxial growth with Metal-Organic-Chemical-Vapor-Deposition (MOCVD), usually performed at near 1000℃ and Ohmic contact formation with Rapid-Thermal-Annealing (RTA) at 880℃ for a conventional metal stack.

Ex-situ AlGaN layer regrowth [1]

This semiconductor interface conditioning approach was reported by our group in Applied Physics Express publication. The method of regrowth itself stems from the research of Prof. Yamamoto [2-4] on normally-off recessed gate AlGaN/GaN HEMTs. Conventionally gate recess structure is created by ICP-RIE with Cl_2 and BCl_3 gas mixture and the process is relatively well understood [5]. However, Reactive Ion Etching causes damage to the surface and AlGaN regrowth was one of the methods to mitigate that. As a result of that treatment devices with strongly positive V_{th} and high I_{Dmax} were reported [6].

At the time, however, no reports were made on the effects of such treatment on non-recessed devices. Our work adapts the trench regrowth method to planar devices.

Device manufacturing: Regrowth with MOCVD

For the most part, process discussed in Chapter 3 was used, however for Regrown AlGaN Surface (RAS) devices MOCVD treatment was performed after wafer dicing but before mesa-etching.

MOCVD treatment we employed was slightly different from mass-production approach [7], as it utilizes lower temperature (<950℃) thus offers lower growth rate. Silicon dioxide coated carbon susceptor with the sample placed in the center is depicted on Figure 1. Central device is constrained with sacrificial sapphire wafers to prevent movement. Reactor chamber is the original development of Prof. Yamamoto and its construction is slightly different from conventional horizontal thermally pre-cracked ion supplied reactor. Both MO precursors are supplied through showerhead portion on the top, as can be seen

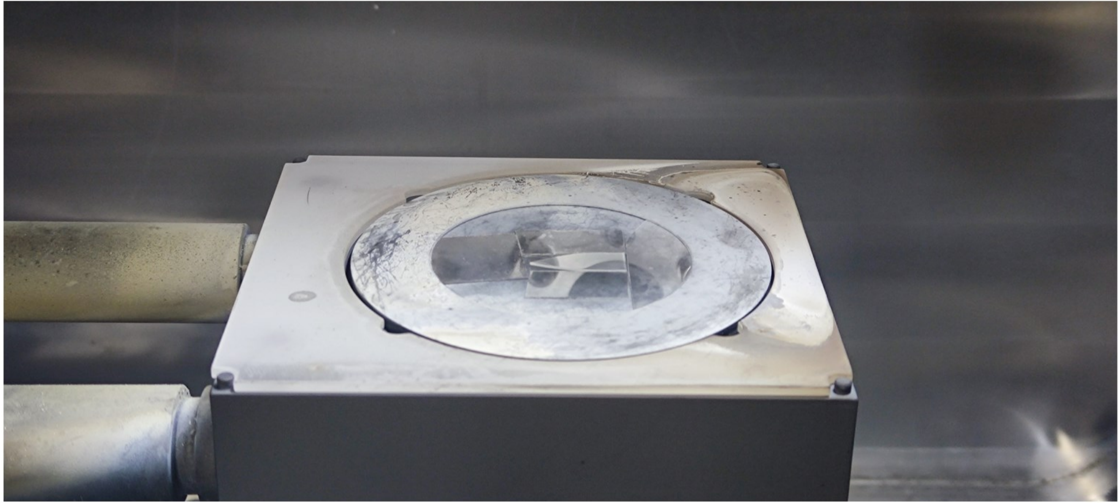


Figure 1. Cleaned wafer on carbon susceptor.

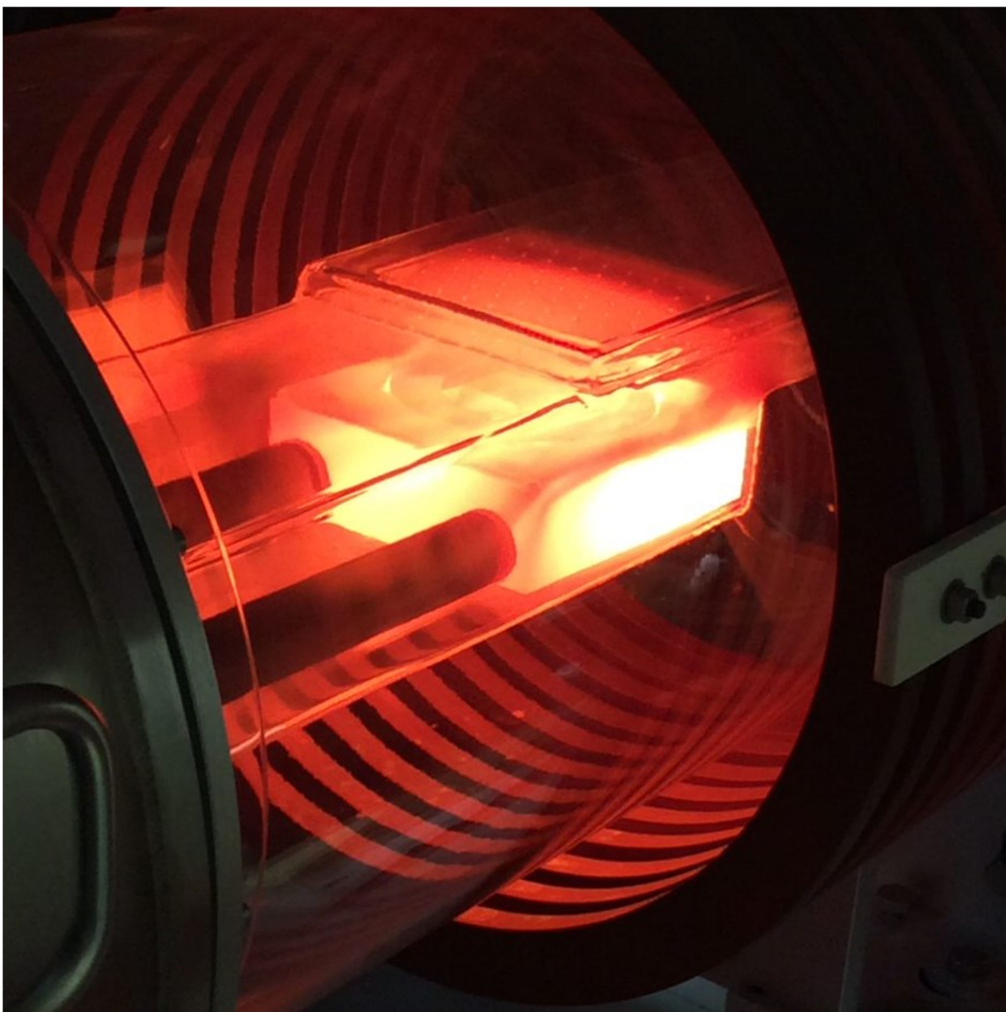


Figure 2. Microwave heated susceptor inside reaction chamber.

on Figure 2. Ammonia is not pre-heated and also separated from the precursor with a controllable flow of nitrogen, injected in between. This inhibits adduct formation and allows for lower growth temperatures. In total, 3 nm thick $Al_{0.25}Ga_{0.75}N$ layer was grown on top of original 24 nm thick layer of the same Al composition.

Further device processing was identical for RAS and reference devices. Finalized device structures are depicted on Figure 3.

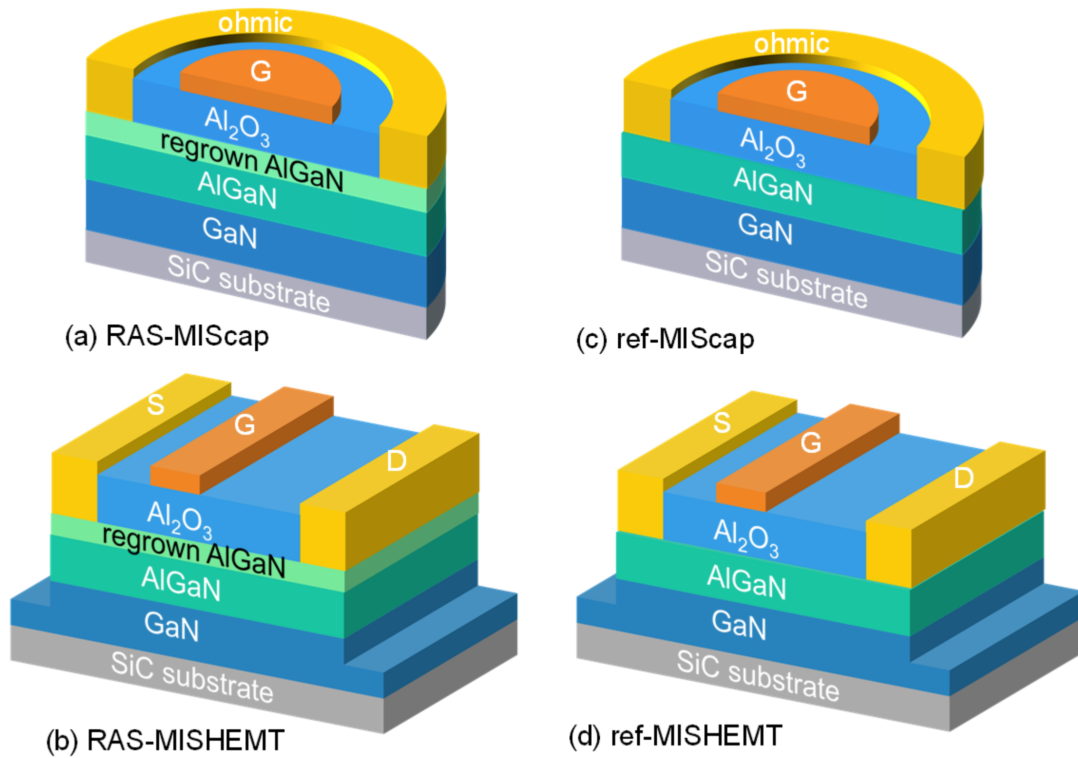


Figure 3 Fabricated devices [1].

Devices (a) and (c) are MIS-Capacitors and (b) and (d) are MIS-HEMTs. MIS-HEMTs device dimensions were W_G = 100 um, L_G = 5 um, L_{GD} = 10 um and L_{GS} = 4 um.

Resulting electrical characteristics and analysis

First, C-V curves of both types of devices were measured, as represented with dots on Figure 4. Due to dielectric breakdown concerns overdrive voltage was limited, so the C-V curve numerical fitting based on DIGS model (as discussed in Chapter 2) was employed to calculate complete C-V curves represented as a

solid line. Some observation can be made from the graph, as pronounced “spill-

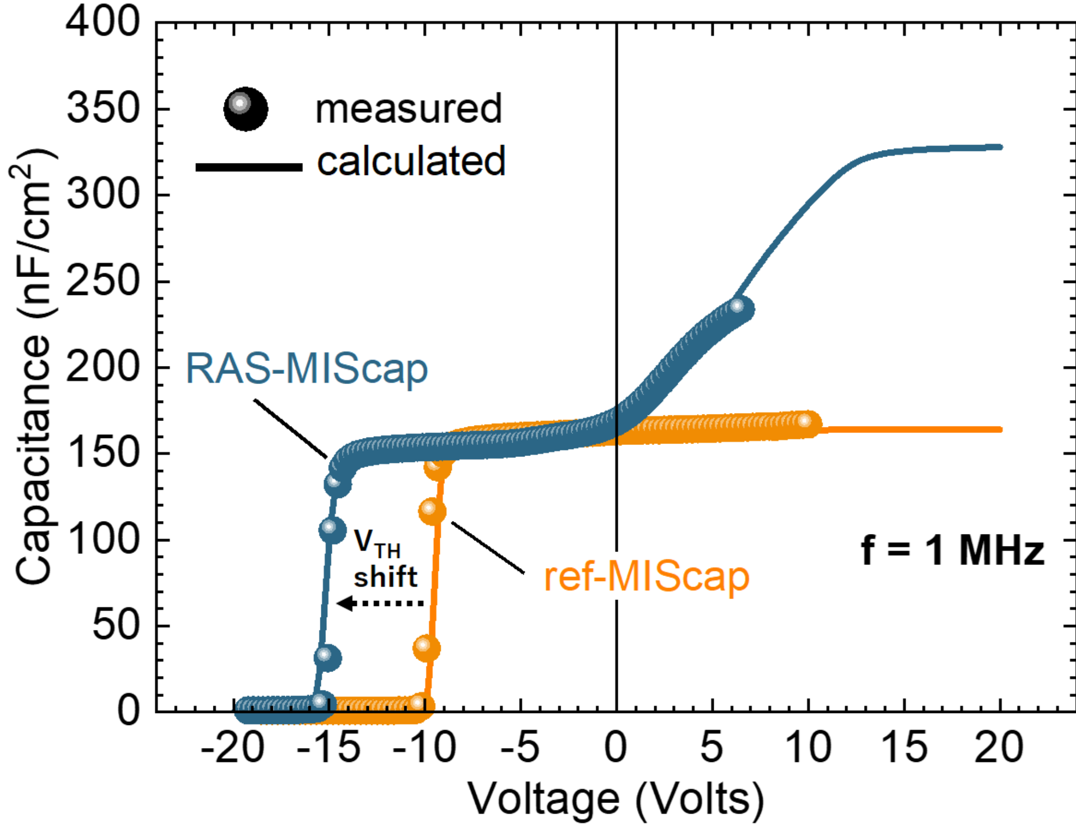


Figure 4. Measured and calculated C-V characteristics

over” for RAS device as well as plateau capacitance value decrease due to extra 3nm of regrown AlGaN on the surface.

At the same time substantial negative threshold voltage shift is also observed. Mathematical model of V_{th} was presented previously [6,8], so equation (1) can be obtained:

$$\frac{d(V_{th})}{d(d_{AlGaN})} = -\frac{d_{AlGaN}}{\epsilon_{AlGaN}} Q_{pol}^{+} \quad (1)$$

where d_{AlGaN} is the original thickness of AlGaN, Q_{pol}^{+} is the cumulative charge at the MIS interface (spontaneous plus piezoelectric polarization charge) and ϵ_{AlGaN} is the dielectric permittivity.

From that, AlGaN layer thickness related shift in threshold voltage would be calculated with (2)

$$\Delta V_{th} = -\left(\frac{d_{AlGaN}}{\epsilon_{AlGaN}} Q_{pol}^{+}\right) \Delta d_{AlGaN} \quad (2)$$

which would yield ΔV_{th} of approximately -0.47 V, if □AlGaN = 9.5□0 and Q_{pol}^{+} = 0.0128 Coul/m^2 were assumed [9]. This result is almost an order of magnitude lower than measured, which indicates another explanation.

Similar to DIGS model C-V curve fitting on Figure 4, DIT extraction was also performed [10,11]. Results for reference and regrown devices can be seen on Figure 5.

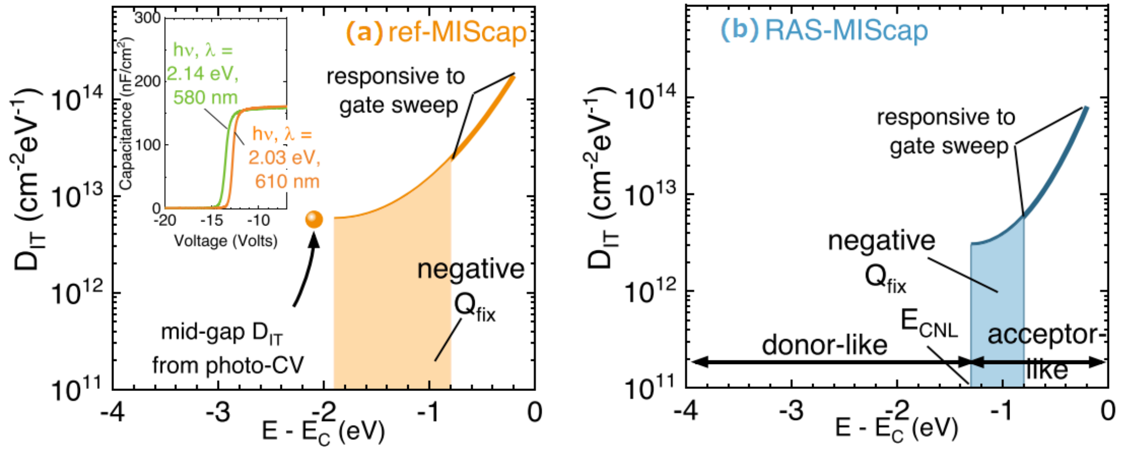


Figure 5. Extracted DIT for reference (a) and RAS (b) devices

While numerical extraction above is definitive for regrown sample due to apparent spill-over in the C-V characteristic, more data points had to be obtained for reference device via Photo-assisted CV measurements [12].

With precise knowledge of interface state distribution, we can further analyze the threshold voltage shift. SRH statistics [13, Chapter 2], trapped charge de-trapping time can be estimated as follows

$$\tau = \frac{1}{v_{th} N_C \sigma_n} e^{\frac{E_T}{kT}} \qquad (3)$$

where v_{th} is the thermal electron velocity, N_C is the effective density of states at the conduction band edge E_C and σ_n is the average capture cross-section of the interface states [25].

Resulting approximate time constant at 300K is in the ballpark of 10^{15} to 10^{20} seconds, which practically means that captured charge deeper than 0.8eV [12] will never de-trap during operation and will be referred as "frozen charge" Q_{it_fr} from now on. It can be calculated from D_{it} distribution by integration over energy as follows: $Q_{it_fr} = -q \int_{E_{CNL}}^{0.8\ eV} D_{it}\, dE$ (4)

Difference in frozen charges in reference and regrown devices can be divided by unitary charge and yields approximately -4.9 V of difference. This matches observed V_{th} shift perfectly

Summarizing Capacitance-Voltage characteristics, we observed lack of spill-over for reference devices, which is expected for samples with higher D_{it} [14,15]. This was consistent with negative V_{th} shift which was explained with decrease in frozen charge at the interface.

Finally, we can turn our attention to DC characteristics of fabricated HEMTs.

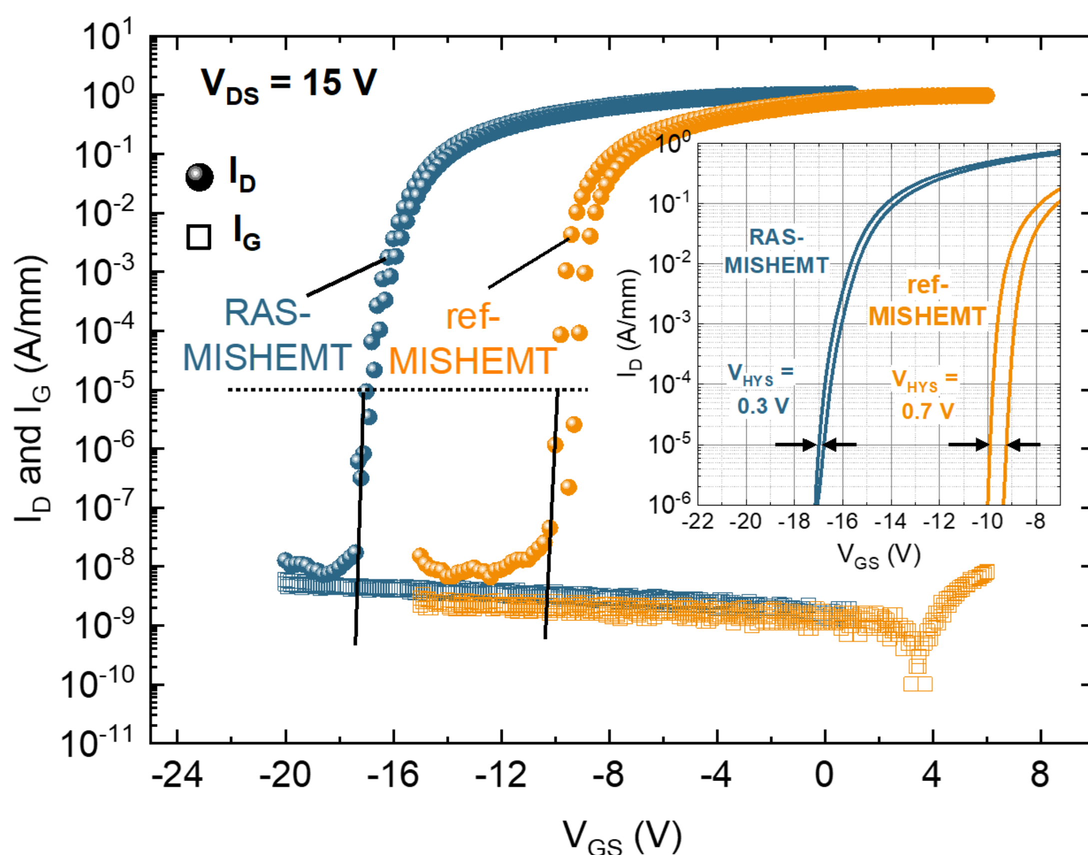


Figure 6. Transfer curve on a logarithmic scale

Transfer curves for both types of fabricated devices are depicted on Figure 6 above. From that we can verify the same threshold voltages as captured on C-V characteristics as well as increased hysteresis in reference device, which is also consistent with D_{it} increase. Overdrive voltages (V_{max}-V_{th}) were matched for fair comparison.

On a linear scale transfer characteristic, depicted on Figure 7 we can observe

drain current and transconductance g_m plotted on the same graph. When threshold voltage is aligned (Figure 7, part b) difference in I_{D_sat} can be clearly

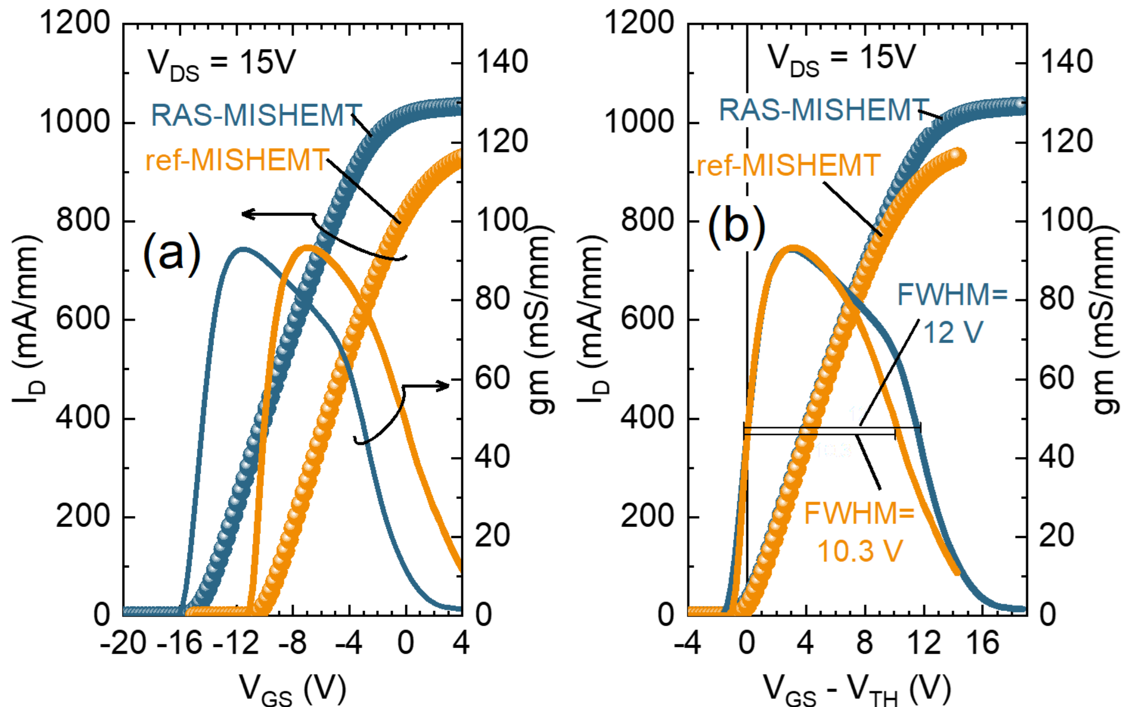


Figure 7. Linear scale transfer characteristics as measured (a) and V_{th} aligned (b) for ease of comparison.

observed, as well as increase in Full-Width-Half-Maximum (FWHM) of transconductance which are important metrics of device performance.

Low thermal budget ohmic contact formation [16]

Findings on low thermal budget process were reported by our group in Japanese Journal of Appled Physics. While MOCVD treatment was focused on removing defects from commercially available epitaxialy grown wafers, this approach aims to prevent damage to the wafer by Rapid Thermal Annealing during ohmic contact formation.

Standard process for ohmic contact formation, discussed in Chapter 3, utilizes Titanium based metal stack and requires relatively high annealing temperature almost approaching 900℃. For this research we used low thermal budget V-based ohmic stack, which was reported previously for high Al content AlGaN layers [17-20]. However, annealing temperature impact on the density of interface

states for MIS structures was never reported previously.

Device manufacturing: V-based Ohmic contact

For manufacturing, standard procedure was followed. Special care was put into processing devices at the same time with minimal handling differences. This was done not to obscure the difference in D_{IT} imparted by annealing temperature with other parameters. Mesa etching, insulator deposition, cleaning and Gate deposition were performed at the same chamber at the same time.

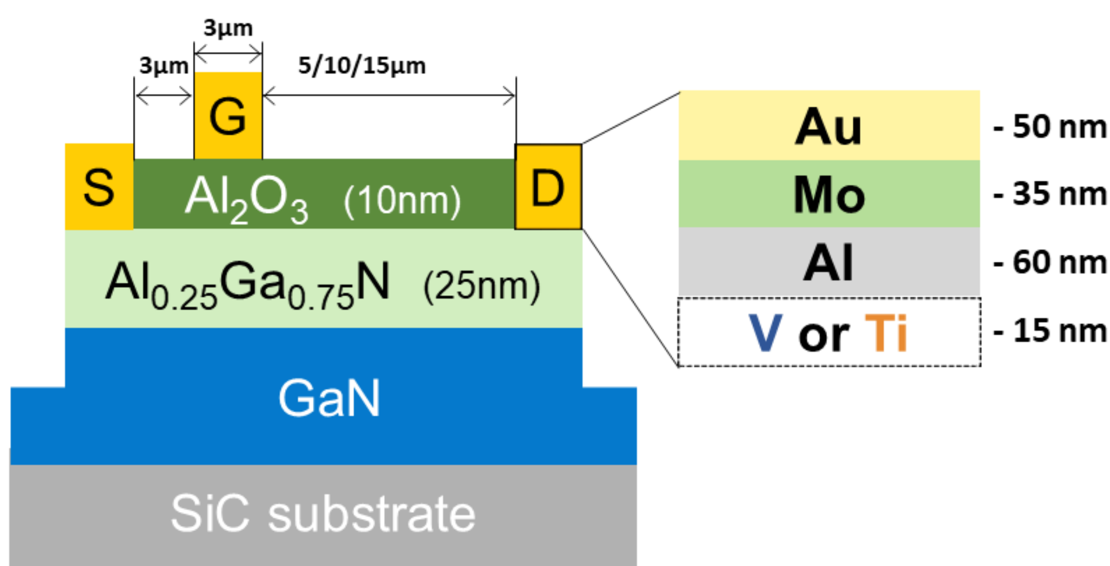


Figure 8. Fabricated device cross-section.

Fabricated devices are depicted on Figure 8. Alongside MIS-HEMTs, MIS-Capacitors and TLM structures were also fabricated.

Resulting electrical characteristics and analysis

First, reference point to previously reported devices [21] had to be established. So our first step was to verify surface morphology, as depicted on Figure 9. Surface of the ohmic contact was examined with Atomic Force Microscopy (AFM) and surface roughness figures we derived. For Ti-based contact, annealed at 880℃, average and RMS roughness was 58.8 and 66.3 nm respectively against 17.5 and 21.3 nm for V-based device annealed at 660 ℃. This correlates pretty well with values reported by Hasegawa et al concerning low temperature

annealing processes. Optical images of TLM patterns are also included in the figure and even visually

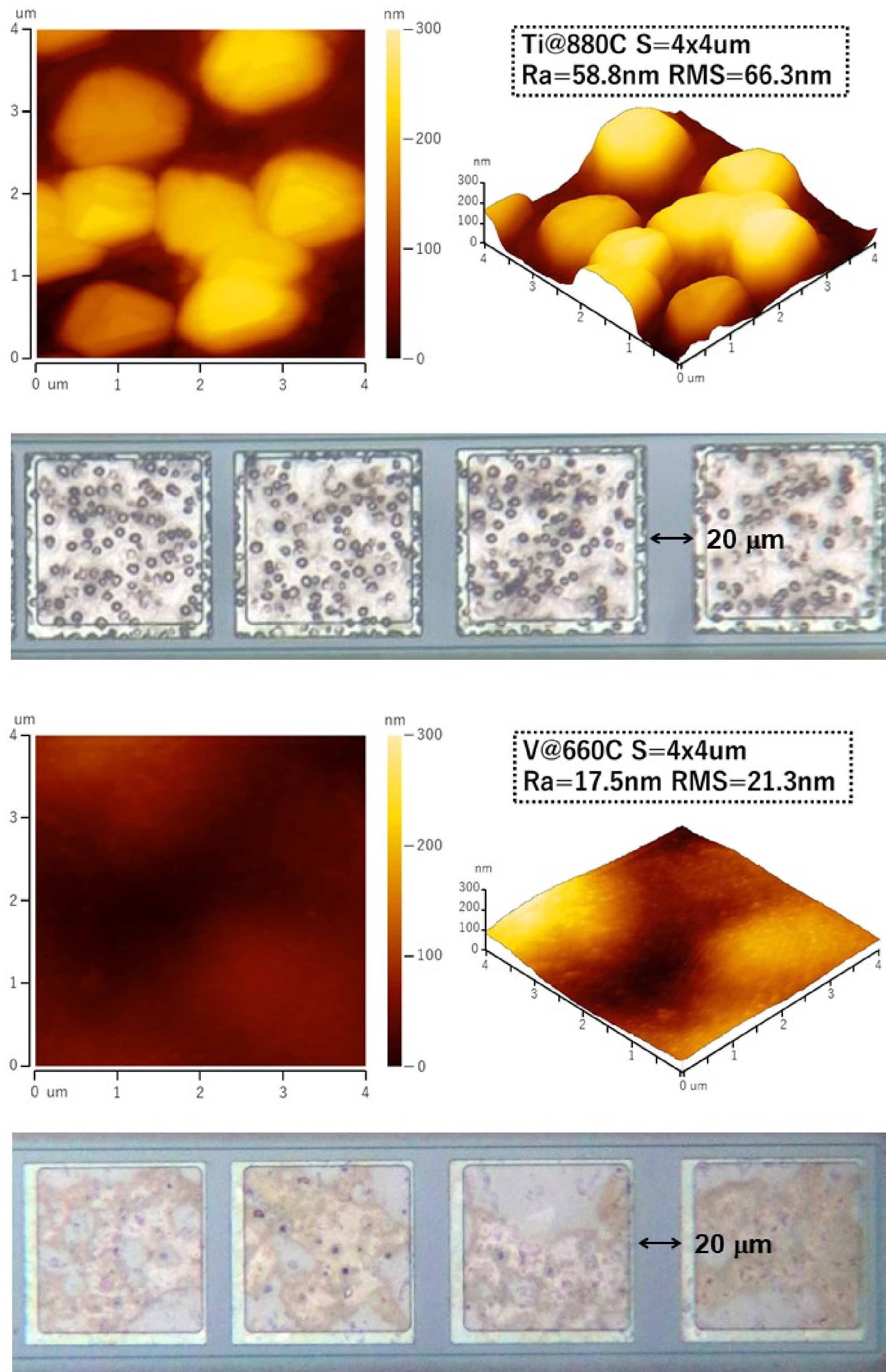


Figure 9. Surface morphology. Ti-based device on top, V-based on the bottom.

Ti-based devices appear to have rougher surface, which is also consistent with reports mentioned above.

Ohmic contact resistance and linearity was measured by Transfer Length Method (TLM) measurements and results are depicted on Figure 10.

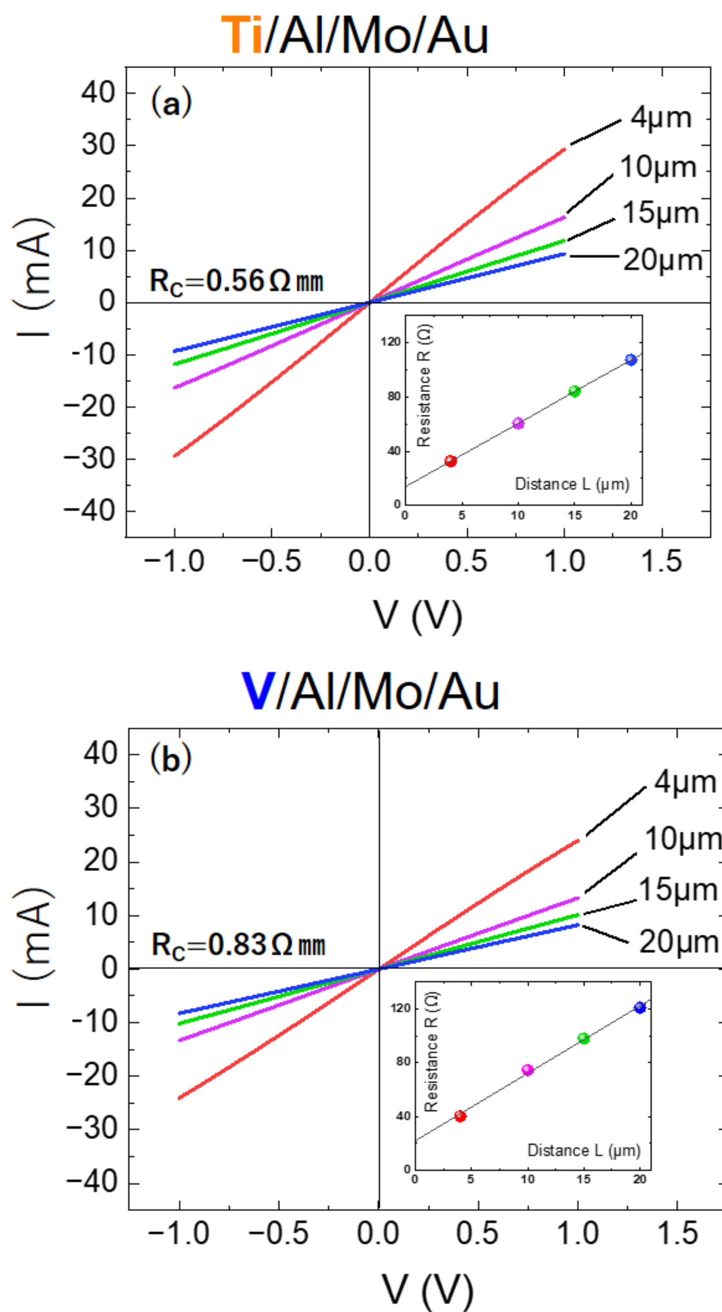


Figure 10. TLM characteristics of the devices

As can be clearly seen, contacts exhibit perfect linearity and more than acceptable contact resistance R_C. R_C value was obtained by method of

intersecting the line on Distance-Resistance graph (insets on Figure 10) with the resistance axis. Absolute values were 0.56 Ωmm For Ti-based devices and 0.83 Ωmm for V-based ones.

The next measurement performed is DC transfer curves of HEMTs, results depicted of Figure 11 in logarithmic scale for V_{DS} = 1 V to observe off-state current and threshold voltage and linear scale on Figure 12 to observe saturation current

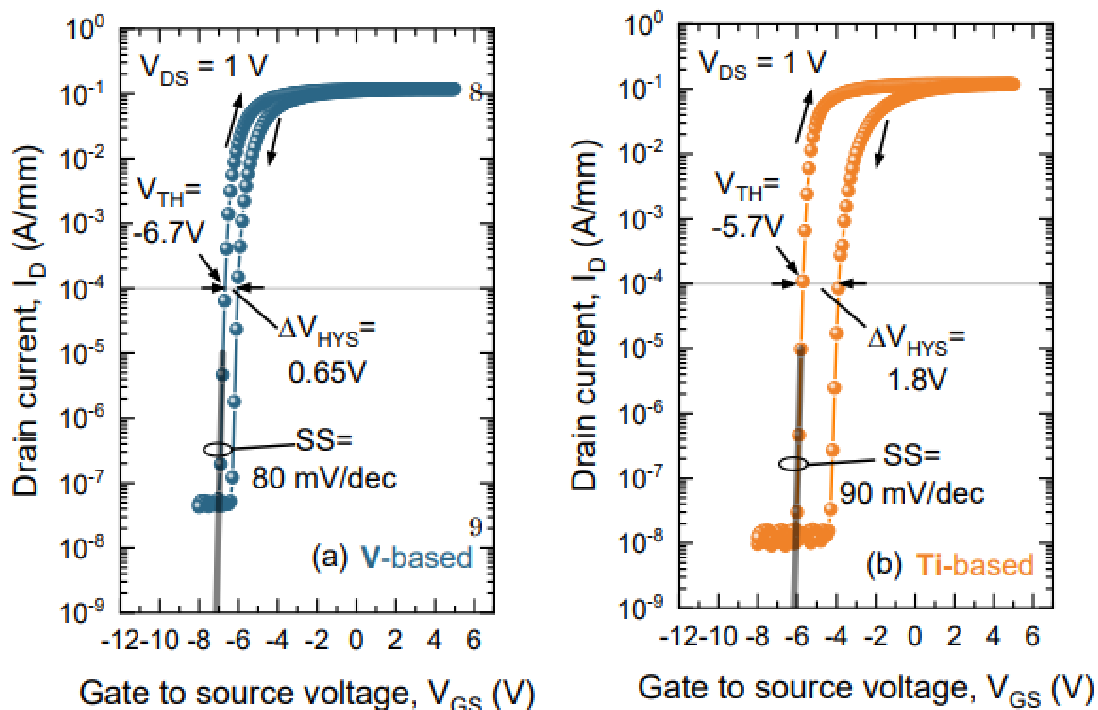


Figure 11. Log-scale transfer curves of HEMTs.

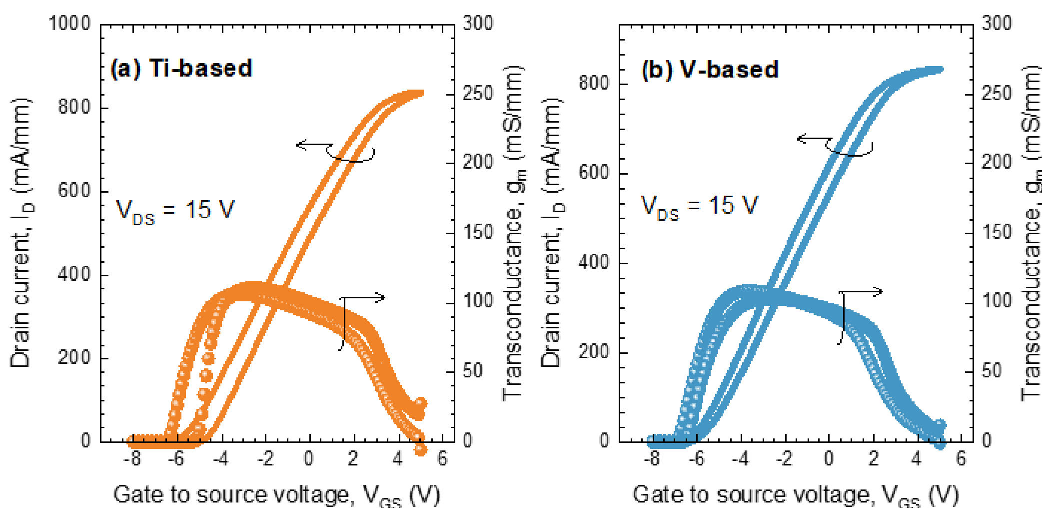


Figure 12. Transfer curves of HEMTs.

and transconductance g_m.

We can clearly see from log. scaled data on Figure 11, that V-based device exhibits a few telltale signs of D_{it} reduction. Signs are the negative shift of threshold voltage [1], decrease in SS value [22] and decrease in hysteresis [23]. From linear scale transfer curves on Figure 12 we see the increase in saturation voltage and can confirm improved hysteresis as well.

Finally, I_D-V_{DS} curves were measured until saturation of drain current was observed, results depicted on Figure 13.

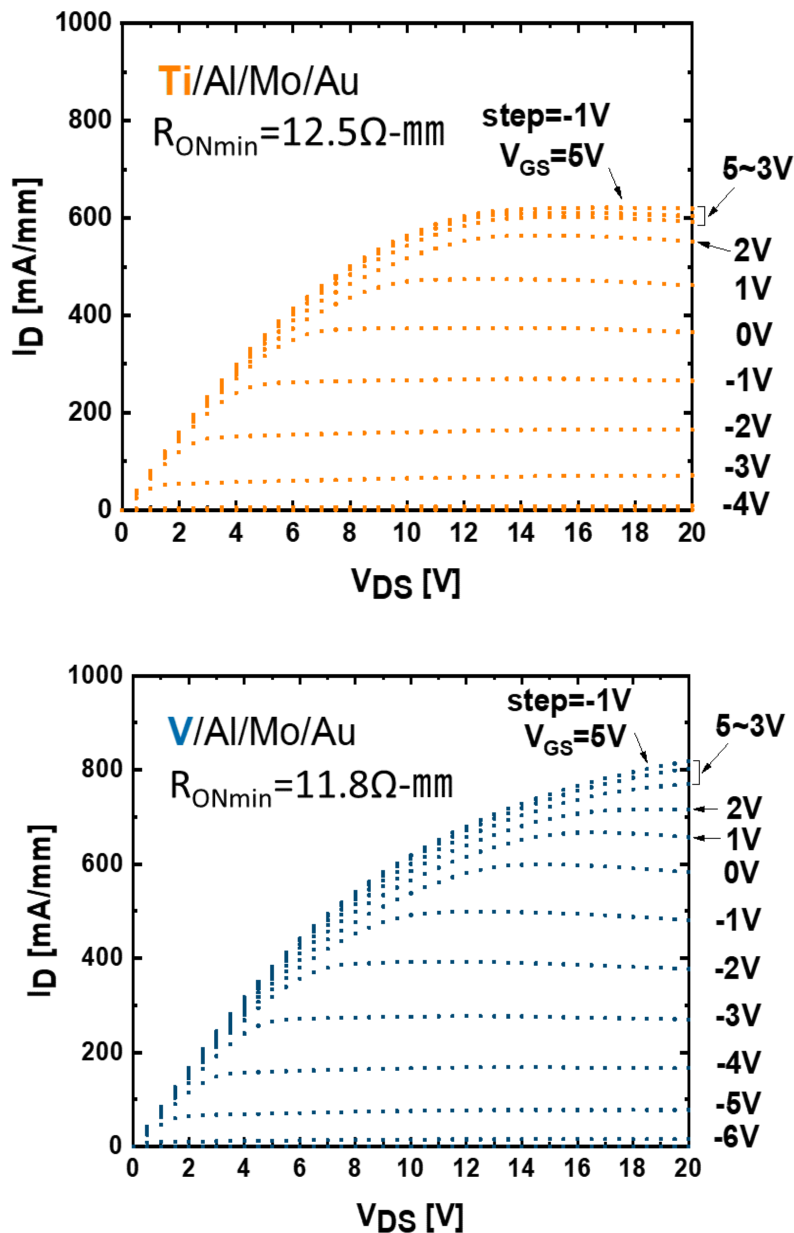


Figure 13. I_D-V_{DS} curves of measured devices.

It can be observed that from V_{GS} = 5 to 3V the current barely changes for both devices, indicating Drain current saturation. However, I_{Dmax} for V-based devices is almost 200 mA/mm larger, indicating significant improvement in interface state density at source and drain access regions. Further proof of that can be derived from ON-resistance [24], which is practically identical for both devices at around 12 Ωmm.

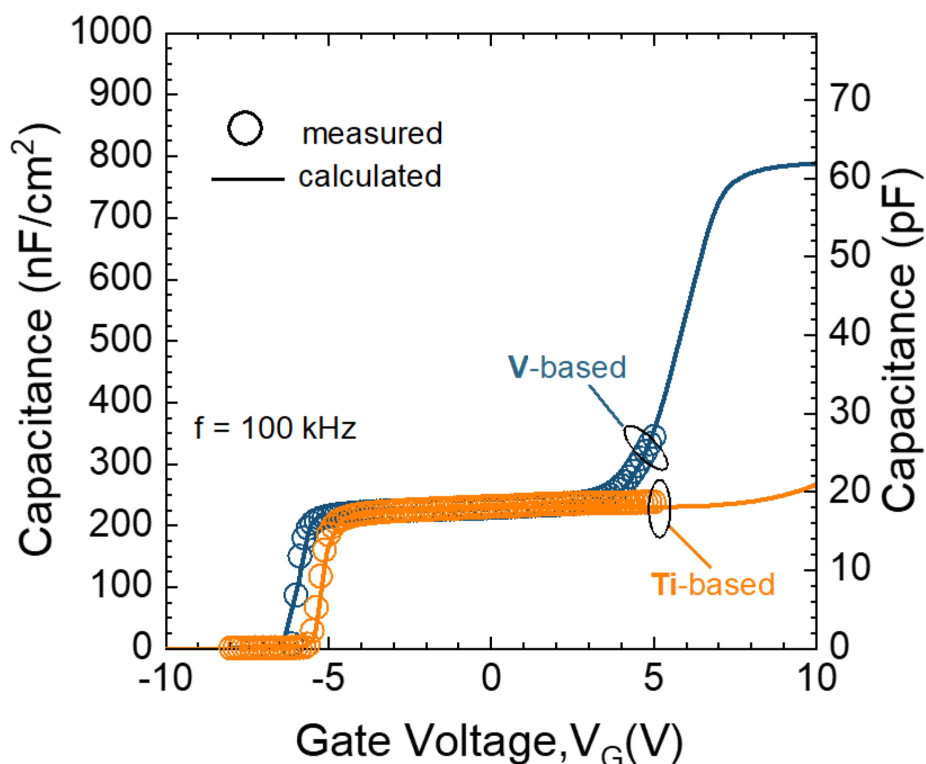


Figure 14. Capacitance-Voltage characteristic of MIS-HEMT

Finally, CV curves were measured for both devices and numerical fitting was also performed, results are indicated on Figure 15.

From measured data we can see pronounced spill-over for V-based device, indicating excellent interface [9, 25, 26]. To further confirm that, Poisson-Schrodinger equation for the device was numerically solved employing DIGS model [9, 27-30] and after rigorous fitting actual D_{IT} distribution was computed. Result shown on Figure 15. We can clearly see that V-based devices exhibit lower interface state density compared to conventional Ti-based counterparts.

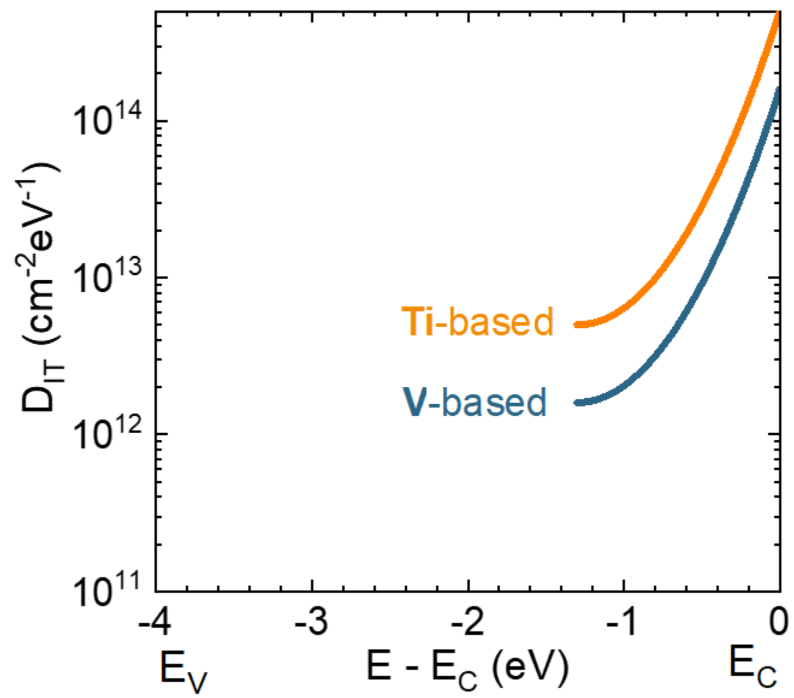


Figure 15. Extracted D_{IT} distributions.

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Chapter 5 Conclusion

Summary

In this research we have explored methods of evaluation and control for Insulator-Semiconductor interface state density in AlGaN/GaN based MIS HEMTs and Capacitor structures.

Two methods, aimed at two highest thermal budget operations in AlGaN/GaN based semiconductor production process were studied. First approach proposes ex-situ MOCVD treatment at non-conventionally low temperatures to passivate and remove surface electronic states. Second approach explores the impact of high temperature Rapid Thermal Annealing during ohmic contact formation on surface state density and suggests low thermal budget ohmic metal stack to be used for improved device performance.

Devices were fabricated and extensively evaluated to confirm interface state density reduction for both proposed methods. During fabrication, special attention was given to simultaneous fabrication of reference devices as well as minimal difference in cleaning and handling methods used. This approach was taken to minimize the impact of other processing steps on the resulting device and avoid obscuring the effects of proposed methods by introduction of unknown variables.

Evaluation and measured impact on device performance

As mentioned above, evaluation focused on both direct and indirect measurement of device performance. Transfer characteristics (I_D-V_{GS}) and drain current curves (I_D-V_{DS}) of a HEMT were evaluated first as they are a direct indicator of device performance in a real-life scenario. To confirm the physical origins of improvement in device characteristics standard and light-assisted MIS capacitor Capacitance-Voltage curve measurements as well as numerical fitting methods were also utilized.

At the same time, other device characteristics like surface morphology, gate capacitance and source/drain contact resistances were carefully monitored to ensure that proposed changes in production process did not impact those in negative or unexpected manner.

For bias and prolonged stress sensitive measurements like C-V or ON-resistance characteristics special care was taken to subject devices to the same

amount of stress time, under and over-drive voltages and illumination conditions. Verification methods include measurement setup automation for accurate and repeatable timing as well as procedures to ensure integrity of measured data across multiple devices.

During the evaluation we have noticed hallmark features of improved insulator-semiconductor interface on devices fabricated with proposed methods and were able to conclusively verify interface improvement with C-V measurements and numerical modelling. Features of improved interface include reduced hysteresis, better subthreshold swing numbers, improved saturation current and dynamic ON resistance. These parameters directly correlate to real-life device performance, which is a strong motivation for incorporating the findings into existing industrial production process.

Impact on manufacturing process

Throughout this work we kept in mind the applied focus of this research and targeted processes with high applicability potential in existing production line conditions.

MOCVD treatment proposed in the research when done ex-situ only adds one step in the production process while imparting no restrictions on consequent treatments or steps of production. This means that it can be incorporated “as is” into existing production lines, with low cost and low time requirements. Moreover, we believe that it has potential to be utilized in in-situ treatment mode, where modified thermal and chemical profiles could be implemented on existing MOCVD growth apparatus for improved results. If implemented this way, it would require no hardware or process flow changes at all, as similar results could be achieved with existing treatment profile modifications.

Low temperature budget ohmic contact formation does not require any changes in the production line at all. Implementation is carried out by the installation of a different metal source in PVD metallization chamber, making this extremely applicable to existing production lines. At the same time, benefits of low thermal budget extend beyond AlGaN/GaN HEMTs and are extremely appealing for precision/yield reasons as well as for combined processes on relatively fragile substrates. For example, combined microchips with GaN-on-Si power amplifier stage and pure Si logic on the same wafer would benefit greatly from such process.

Further work

We have proposed two methods separately, so the most logical next step would be to combine those approaches and extensively study the result. This in turn might give us an insight into the physics of trap distribution and inter-trap interaction during production process. For definitive results more precise trap energy level mapping apparatus will have to be designed and more surface focused measurements like TEM or AES might be required.

Some work on individual method optimization can be also performed. MOCVD treatment profile optimizing and careful temperature/process chemical control might lead us to more efficient in-situ growth recipes. This is especially promising in recessed normally-OFF HEMTs, where increase in saturation current is even more important due to threshold voltage to current trade-off.

Ohmic contact formation and optimization is a whole separate field by itself, but our work describing the impact of low temperature budget on surface states might inspire new research efforts towards another low temperature ohmic contact formation approaches.

Finally, gate oxide deposition method itself is the next sensible target for this research, as its impact on surface states was demonstrated by multiple groups including ours. Surface treatment inevitably occurs during oxide deposition, but its type and extent vary greatly depending on the deposition method. More sophisticated surface inspection and interface simulation tools might need to be developed for robust understanding of underlying physics.

List of Abbreviations

SiC – Silicon Carbide
GaN – Gallium Nitride
MESFET – MEtal Semiconductor Field Effect Transistor
HBT – Hybrid Bypolar Transistor
HEMT – High Electron Mobility Transistor
AlGaN – Aluminum Gallium Nitride
2DEG – Two Dimensional Electron Gas
SG – Schottky Gate
MIS – Metal Insulator Semiconductor
DIGS – Disorder Induced Gap State
ICP – Inductively Coupled Plasma
RIE – Reactive Ion Etching
CVD – Chemical Vapour Deposition
*D*it – Density of Interface States
SS – Subthreshold Swing
DUT – Device Under Test
NDR – Normalized Dynamic Resistance
QSCV – Quasi-Static Capacitance Voltage
CWCV – Continuous Wave Capacitance Voltage
SRH model – Shockley-Read-Hall model
RTA – Rapid Thermal Annealing
ALD – Atomic Layer Deposition
TMA – Trimethylaluminium
RF – Radio Frequency
MOCVD – Metal Organic Chemical Vapor Deposition
TLM – Transfer Length Method

List of Publications

Peer reviewed journal publications:

○[1] **Ali Baratov**, Shinsaku Kawabata, Shun Urano, Itsuki Nagase, Masaki Ishiguro, Shogo Maeda, Takahiro Igarashi, Toi Nezu, Zenji Yatabe, Maciej Matys, Tetsu Kachi, Boguslawa Adamowicz, Akio Wakejima, Masaaki Kuzuhara, Akio Yamamoto, and Joel T. Asubar, Appl. Phys. Express 15, 104002 (2022).

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